ME 333 Assignment 5

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1 The PIC32 ADC Peripheral

(a) The processor runs at 80 MHz, or alternatively, 80 megacycles per second. Timer 3 counts from one to eight with a prescaler value of two, so it takes $8 * 2 = 16$ cycles for the wait loop to end. Dividing this by the processor speed, we get $16 \frac{cycles}{loop} / 80 \frac{megacycles}{sec} = 200ns$, which as expected, is greater than 132ns.

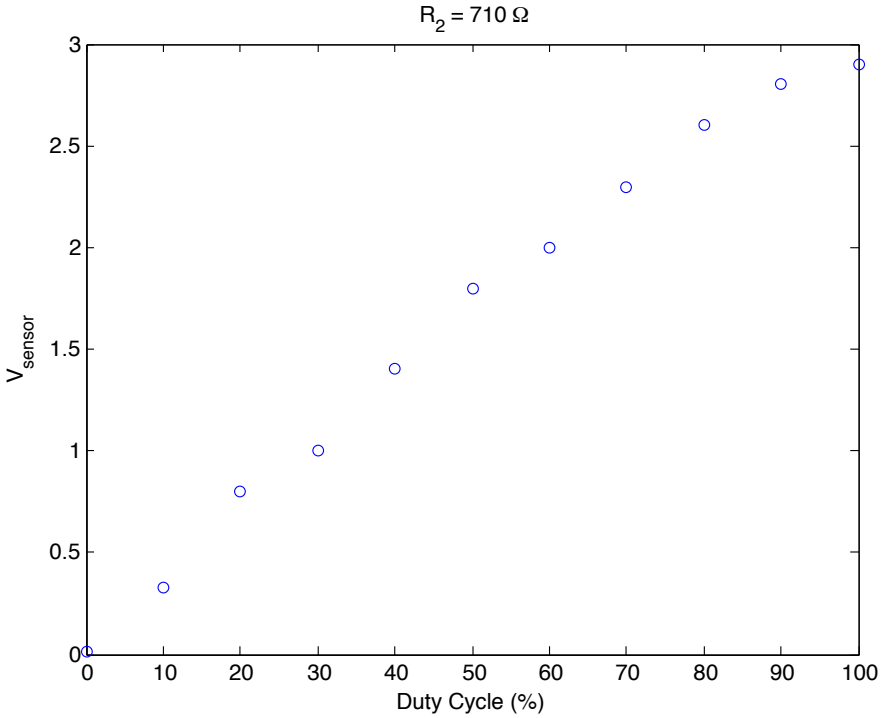

Figure 1: It begins to level off around 90%, but even so, there is still measurable increase in voltage.

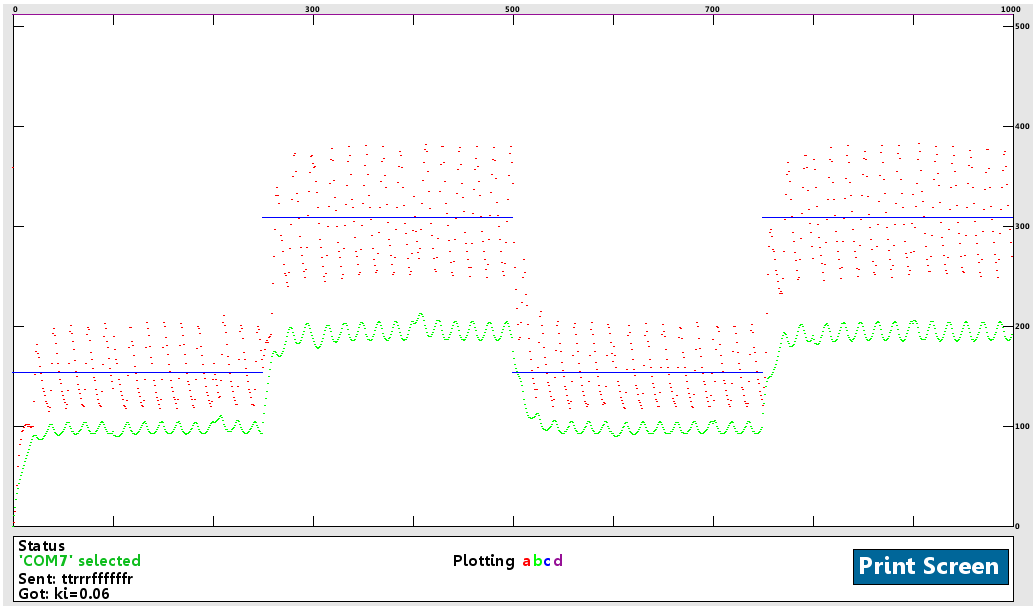

Figure 2: Results of control law. The red line (analog input reading) generally matches with desired voltage(blue line). However the reading jumps around a lot, a result of not having a large enough capacitor.

(c) $K_p = .02$, $K_i = .06$