

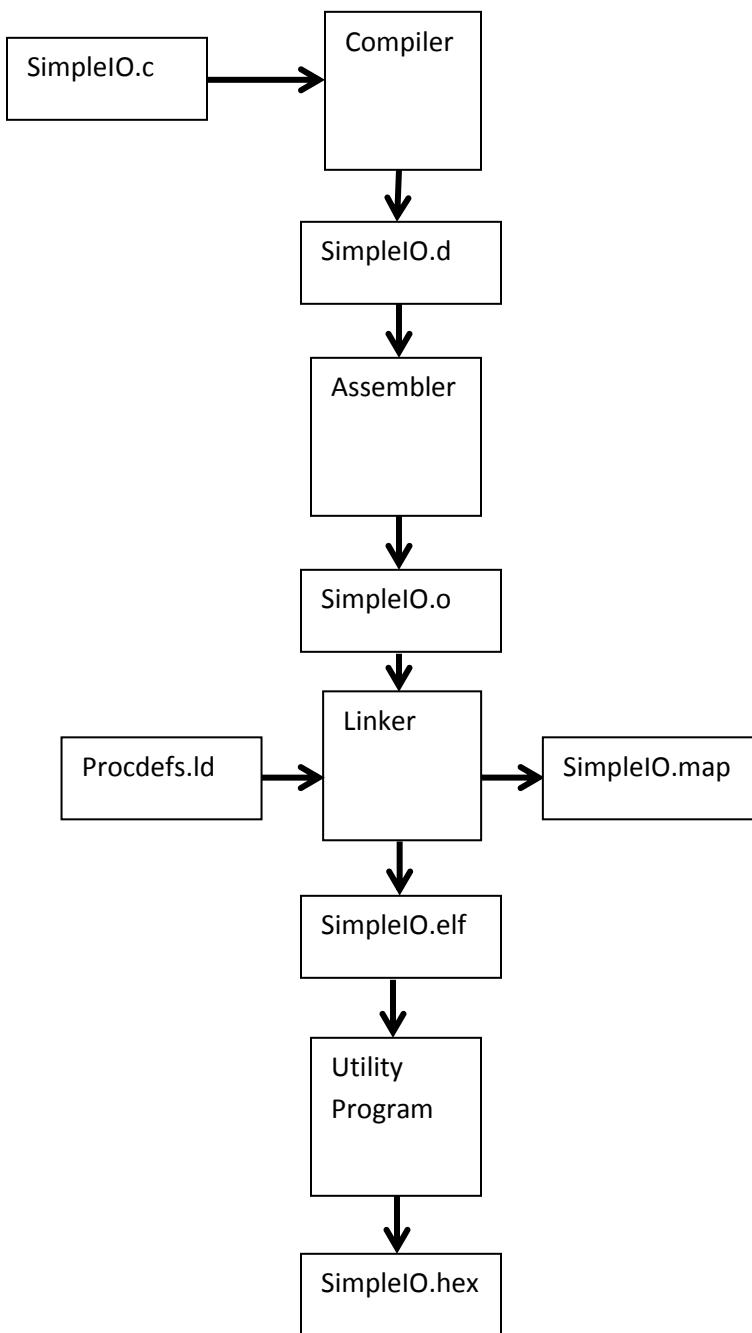
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Assignment 3
Mechatronics

(a)

Compiling the C code generated the following files:

SimpleIO.elf
SimpleIO.hex
SimpleIO.map
SimpleIO.o
SimpleIO.d

(b)



1.2

(c)

Compiler - pic32-gcc.exe
Assembler - pic32-as.exe
Object Linker - pic32-ld.exe

(d)

C:\Program Files (x86)\Microchip\MPLAB C32 Suite\bin
pic32-addr2line.exe
pic32-ar.exe
pic32-as.exe

1.3

(a)

0x9d001818 main
0x9d001bac delay

(b)

SimpleIO.o is 0x3e4 = 996 bytes.

(c)

Memory footprint of SimpleIO.o is 0x570 = 1392 bytes.

There is a difference of 396 bytes. Other additional functions are written into the .text file that allows simpleIO.o to run.

1.4

(a)

TRISGCLR =0x3000 generates 3 lines of assembly code.
TRISG &= 0xCFFF generates 5 lines of assembly code.

(b)

Optimization level zero both is slower and takes up more memory than optimization level 3.

Optimization level 0- 485 bytes program memory. 1024 bytes data memory.

Actual Function—20 lines

```
42:          void delay(int n) {  
 9D001BFC 27BDFFFF addiu    sp,sp,-16  
 9D001C00 AFBE0008 sw       s8,8(sp)  
 9D001C04 03A0F021 addu    s8,sp,zero  
 9D001C08 AFC40010 sw       a0,16(s8)  
 43:          int i;  
 44:          for(i = 0; i < n; i++);  
 9D001C0C AFC00000 sw       zero,0(s8)  
 9D001C10 8FC20000 lw       v0,0(s8)  
 9D001C14 8FC30010 lw       v1,16(s8)  
 9D001C18 0043102A slt      v0,v0,v1  
 9D001C1C 10400006 beq      v0,zero,0x9d001c38  
 9D001C20 00000000 nop  
 9D001C24 8FC20000 lw       v0,0(s8)  
 9D001C28 24420001 addiu   v0,v0,1  
 9D001C2C AFC20000 sw       v0,0(s8)  
 9D001C30 1000FFF7 beq      zero,zero,0x9d001c10  
 9D001C34 00000000 nop  
 45: }
```

```

9D001C38 03C0E821 addu    sp,s8,zero
9D001C3C 8FBE0008 lw      s8,8(sp)
9D001C40 27BD0010 addiu   sp,sp,16
9D001C44 03E00008 jr     ra
9D001C48 00000000 nop

```

Optimization level 3- 390 bytes program memory. 1024 bytes data memory.

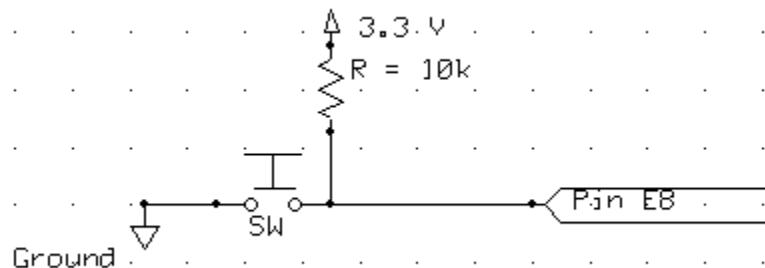
Actual Function—8 lines

```

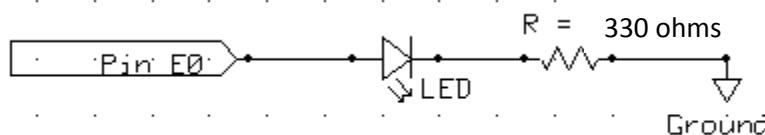
42:     void delay(int n) {
43:         int i;
44:         for(i = 0; i < n; i++);
9D001A74 18800005 blez    a0,0x9d001a8c
9D001A78 00001821 addu    v1,zero,zero
9D001A7C 24630001 addiu   v1,v1,1
9D001A80 0064102A slt     v0,v1,a0
9D001A84 5440FFFE bnel    v0,zero,0x9d001a80
9D001A88 24630001 addiu   v1,v1,1
9D001A8C 03E00008 jr     ra
9D001A90 00000000 nop

```

(a)



(b)



(c) Virtual Address BF88_6110

Its default is for all of the pins (0-9) to be set to 1 – 0x03FF. This corresponds to setting them all to inputs.

No, only the first 10 bits (bits 0-9) of the 32 bit register are relevant.

(d) They are 32 bit locations in memory or registers that are used to set the special functions of the pins in port E. An unsigned int is a 32 bit data type that could be used.

LATE- hold port I/O data

TRISE- configure data direction flow (input or output)

PORTE- allows I/O pins to be accessed

(e) Writing to LATE for example, LATE = 0x00FF, sets the digital output for port e. Reading from PORTE, for example, val = PORTE, returns the current digital state of port e. They are the same in that writing to PORTE is the same as writing to LATE. However, reading from LATE gives the value held in the PORTE data latch, and does not read the current value of the I/O pins.

(f) Line 40069 of p32mx795f512l.h defines the memory address of PORTE.

```
#define _PORTE_BASE_ADDRESS 0xBF886100
```