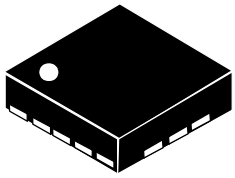
ASM330LXH

Automotive inertial module: 3D accelerometer and 3D gyroscope

Datasheet - preliminary data



LGA-16L (3x3x1.1mm)

Features

- Analog supply voltage: 2.0 V to 3.6 V
- Independent IOs supply (2.0 V) and supply voltage compatible
- Power-down and sleep modes
- 3 independent acceleration channels and 3 angular rate channels
- ±2/±4/±8/±16 *g* selectable full scales
- ±125/±245/±500/±1000/±2000 dps selectable full scales
- SPI/I^2C serial interface
- Embedded temperature sensor
- Embedded FIFOs
- ECOPACK® RoHS and “Green” compliant
- AEC-Q100 qualification

Applications

- GPS-assisted car navigation
- Telematics, eTolling
- Anti-theft systems
- Impact recognition and logging
- Motion-activated functions
- Vibration monitoring and compensation
- Appliances and robotics

Description

The ASM330LXH is a system-in-package featuring a 3D digital accelerometer and a 3D digital gyroscope. ST’s family of MEMS sensor modules leverages the robust and mature manufacturing processes already used for the production of micromachined accelerometers and gyroscopes.

The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are developed using CMOS technology that allows the design of a dedicated circuit which is trimmed to better match the characteristics of the sensing element.

The ASM330LXH has a user-selectable full scale acceleration range of ±2/±4/±8/±16 *g* and an angular rate range of ±125/±245/±500/±1000/±2000 dps. The ASM330LXH has two operating modes in that the accelerometer and gyroscope sensors can be either activated at the same ODR or the accelerometer can be enabled while the gyroscope is in power down.

The ASM330LXH is available in a plastic land grid array (LGA) package.

Table 1. Device summary

Part number	Temp. range [°C]	Package	Packing
ASM330LXH	-40 to +85	LGA-16L (3x3x1.1mm)	Tray
ASM330LXHTR	-40 to +85		Tape and reel

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1 Pin description

Figure 1. Pin connections

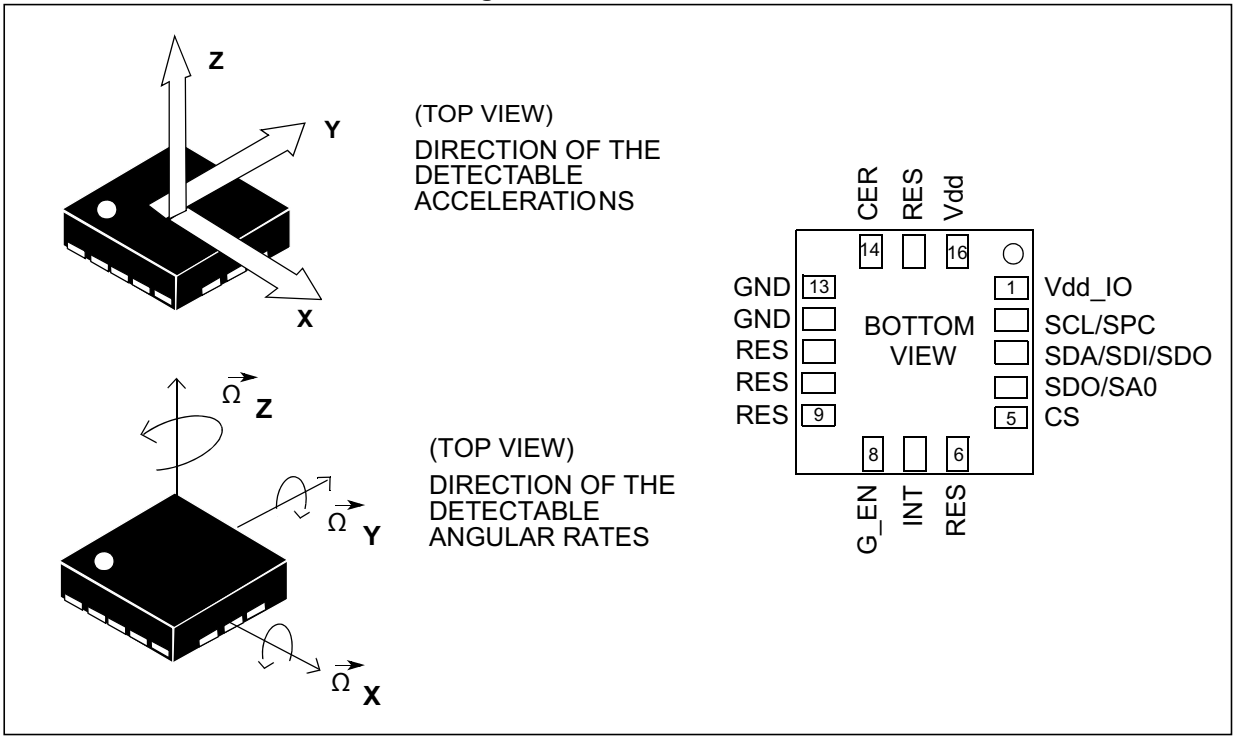


Table 2. Pin description

Pin#	Name	Function
1	Vdd_IO(1)	Power supply for I/O pins
2	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
3	SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
4	SDO SA0	SPI serial data output (SDO) I^2C least significant bit of the device address (SA0)
5	CS	I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
6	RES	Connect to GND
7	INT	Programmable interrupt
8	G_EN	Gyroscope data FIFO sync enable
9	RES	Connect to GND
10	RES	Connect to GND
11	RES	Connect to Vdd or GND

Table 2. Pin description (continued)

Pin#	Name	Function
12	GND	0 V supply
13	GND	0 V supply
14	CER	Connect to GND with ceramic capacitor(2)
15	RES	Connect to Vdd or GND
16	Vdd(3)	Power supply

1. Recommended 100 nF filter capacitor.
2. 10 nF (±10%), 16 V. 1 nF minimum value has to be guaranteed under 12 V bias condition.
3. Recommended 100 nF plus 10 µF capacitors.

2 Module specifications

2.1 Mechanical characteristics

@ Vdd = 3.0 V, T = -40 °C to +85 °C unless otherwise noted [a]

Table 3. Mechanical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.[1]	Max.	Unit
LA_FS	Linear acceleration measurement range			2 4 8 16		*g*
G_FS	Angular rate measurement range			125 245 500 1000 2000		dps
LA_So	Linear acceleration sensitivity	@LA_FS = 2 g		0.061		mg/LSb
		@LA_FS =4 g		0.122		
		@LA_FS = 8 g		0.244		
		@LA_FS =16 g		0.488		
G_So	Angular rate sensitivity	@G_FS =125 dps		4.37		mdps/LSb
		@G_FS = 245 dps		8.75		
		@G_FS = 500 dps		17.5		
		@G_FS = 1000 dps		35		
		@G_FS = 2000 dps		70		
LA_SoDr	Linear acceleration sensitivity change vs. temperature	From -40 °C to +85 °C		0.01		%/°C
G_SoDr	Angular rate sensitivity change vs. temperature	From -40 °C to +85 °C		0.01		%/°C
LA_TyOff	Linear acceleration zero-*g* level accuracy[2][3]			30		m*g*
G_TyOff	Gyroscope zero-rate level accuracy[2][3]			10		dps
LA_TCOff	Linear acceleration zero-*g* level change vs. temperature	From -40 °C to +85 °C		0.05		mg/°C
G_TCOff	Angular rate zero-rate level change vs. temperature	From -40 °C to +85 °C		0.05		dps/°C

a. The product is factory calibrated at 3.0 V. The operational power supply range is from 2.0 V to 3.6 V.

Table 3. Mechanical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
An	Acceleration noise density	LA_FS = 2 *g*		80		$\mu g/(\sqrt{Hz})$
Rn	Rate noise density			0.006		$dps/(\sqrt{Hz})$
ODR	Output data rate	Gyro OFF / ON		800 400 200 100 50 12.5		Hz
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Typical zero-*g* level offset / zero rate offset values after MSL3 preconditioning.
3. Offset can be eliminated by enabling the built-in high-pass filter.

2.2 Electrical characteristics

@ Vdd = 3.0 V, T = -40 °C to +85 °C unless otherwise noted

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
Vdd(2)	Supply voltage		2.0		3.6	V
Vdd_IO(2)	Power supply for I/O		2.0		3.6	V
LA_Idd	Accelerometer current consumption in normal mode	ODR ≥ 100 Hz		245		µA
LA_Idd_LP	Accelerometer current consumption in low-power mode	ODR = 50 Hz		65		µA
		ODR = 100 Hz		115		
LA_G_Idd	Accelerometer and gyroscope current consumption in normal mode			4.3		mA
Idd_PD	Accelerometer and gyroscope current consumption in power down			6		µA
Trise	Time for power supply rising		0.01		100	ms
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Vdd and Vdd_IO can power up in either order.

2.3 Temperature sensor characteristics

@ Vdd = 3.0 V, T = 25 °C unless otherwise noted (b)

Table 5. Temperature sensor characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
TODR	Temperature refresh rate			50		Hz
TSen	Temperature sensitivity			16		LSB/°C
TST	Temperature stabilization time(2)				500	µs
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Time from power on bit to valid temperature data based on characterization data.

b. The product is factory calibrated at 3.0 V.

2.4 Communication interface characteristics

2.4.1 SPI - serial peripheral interface

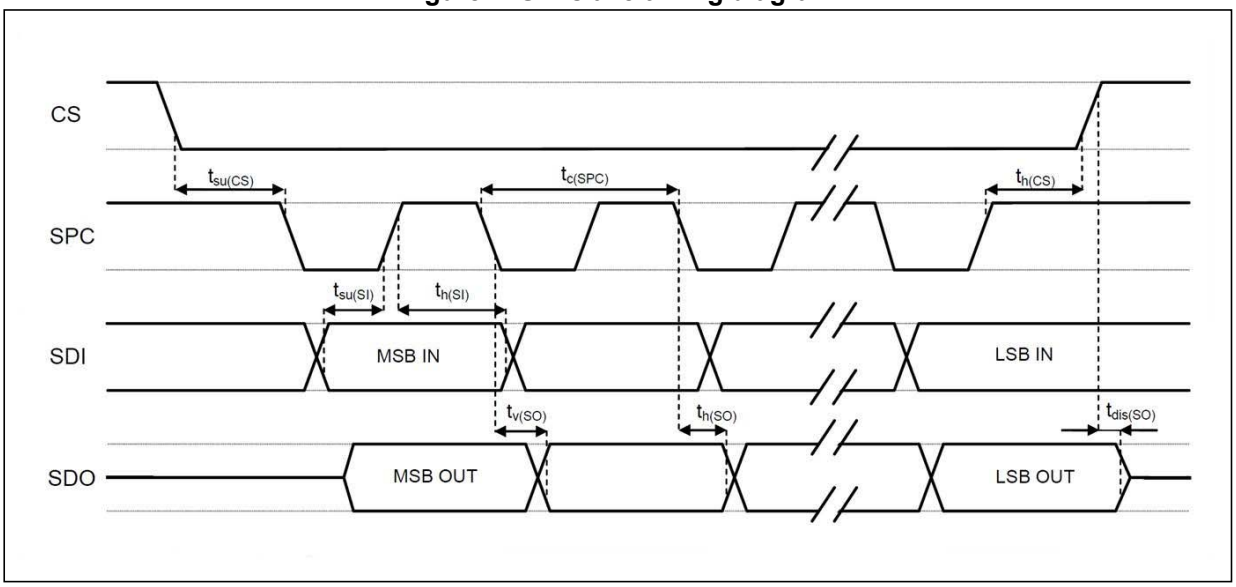
Subject to general operating conditions for Vdd and Top.

Table 6. SPI slave timing values

Symbol	Parameter	Value(1)		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	5		ns
$t_{h(CS)}$	CS hold time	20		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	5		
$t_{dis(SO)}$	SDO output disable time		50	

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production

Figure 2. SPI slave timing diagram



Note: Measurement points are done at 0.2:Vdd_IO and 0.8:Vdd_IO, for both input and output ports.

2.4.2 I²C - inter IC control interface

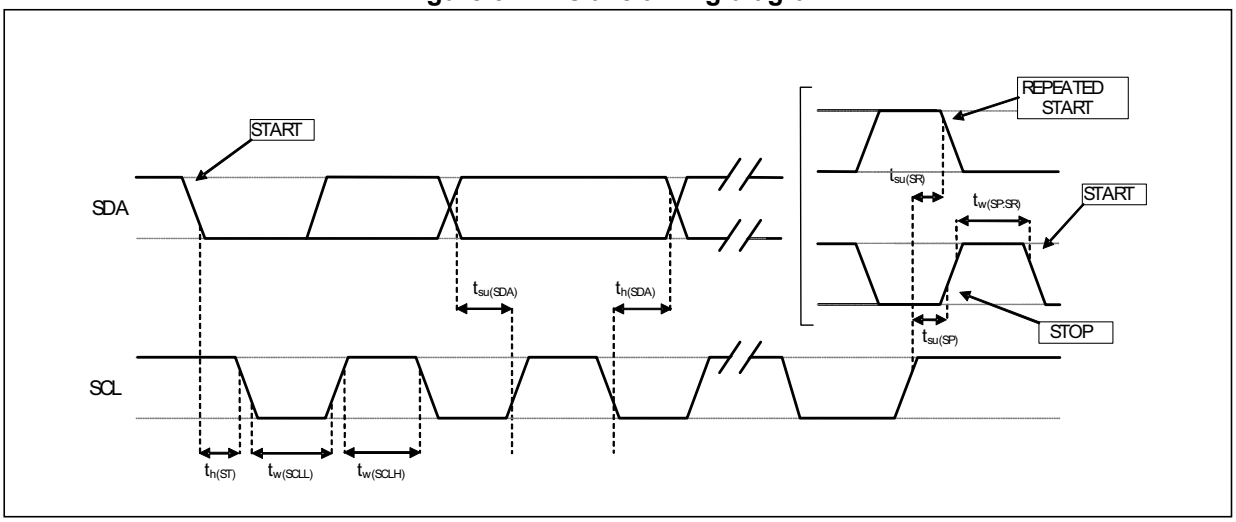
Subject to general operating conditions for Vdd and Top.

Table 7. I²C slave timing values

Symbol	Parameter	I²C standard mode(1)		I²C fast mode (1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0	3.45	0	0.9	µs
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production.

Figure 3. I²C slave timing diagram



Note: Measurement points are done at 0.2:Vdd_IO and 0.8:Vdd_IO, for both ports.

2.5 Absolute maximum ratings

Stresses above those listed as ”Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
T_{STG}	Storage temperature range	-40 to +125	°C
Sg	Acceleration g for 0.1 ms	10,000	*g*
ESD	Electrostatic discharge protection	2 (HBM)	kV
Vin	Input voltage on any control pin (including CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0, G_EN)	0.3 to Vdd_IO +0.3	V

Note: Supply voltage on any pin should never exceed 4.8 V.

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

2.6 Terminology

2.6.1 Sensitivity

Linear acceleration sensitivity can be determined for example by applying 1 *g* acceleration to the device. Because the sensor can measure DC accelerations, this can be done easily by pointing the selected axis towards the ground, noting the output value, rotating the sensor 180 degrees (pointing towards the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and over time. The sensitivity tolerance describes the range of sensitivities of a large number of sensors.

An angular rate gyroscope is device that produces a positive-going digital output for counterclockwise rotation around the axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time.

2.6.2 Zero-*g* and zero rate level

Linear acceleration zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface will measure 0 *g* on both the X-axis and Y-axis, whereas the Z-axis will measure 1 *g*. Ideally, the output is in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as 2’s complement number). A deviation from the ideal value in this case is called zero-*g* offset.

Offset is to some extent a result of stress to MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Linear acceleration zero-*g* level change vs. temperature” in *Table 3: Mechanical characteristics*. The zero-*g* level tolerance (TyOff) describes the standard deviation of the range of zero-*g* levels of a group of sensors.

Zero-rate level describes the actual output signal if there is no angular rate present. Zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time.

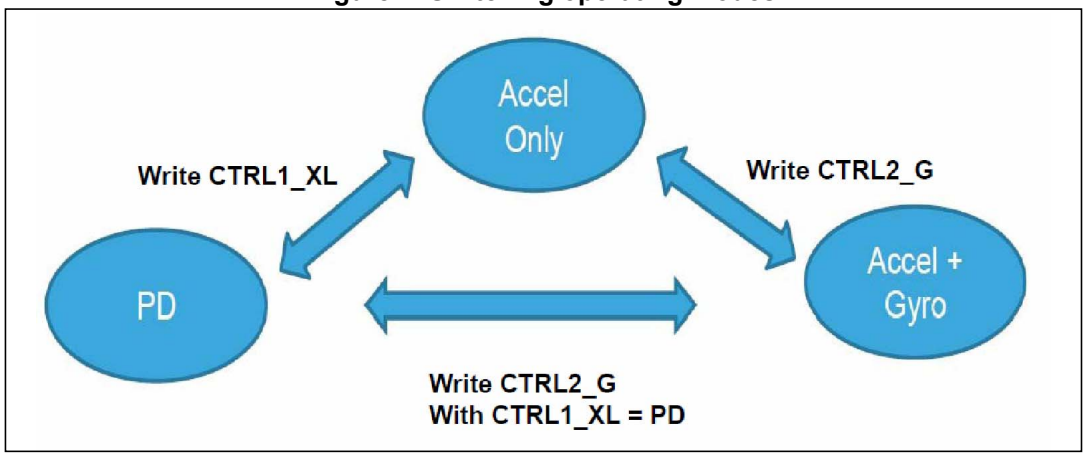
2.7 Functionality

2.7.1 Operating mode

The ASM330LXH has two operating modes available: only accelerometer active and gyroscope in power-down or both accelerometer and gyroscope sensors active at the same ODR. Switching from one mode to the other requires one write operation: writing to *CTRL1_XL (10h)* the accelerometer operates in normal mode and the gyroscope is powered down; writing to *CTRL2_G (11h)* both accelerometer and gyroscope are activated at the same ODR.

For further information in order to enable one operating mode from the power down, please refer to *Figure 4: Switching operating modes*.

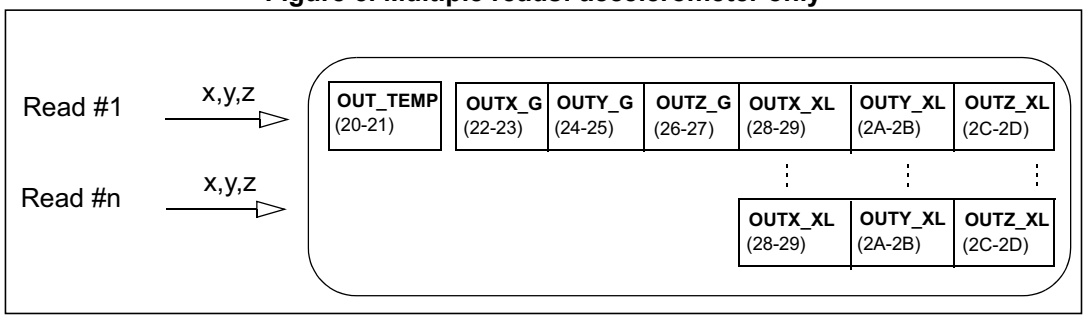
Figure 4. Switching operating modes



2.7.2 Multiple reads (burst)

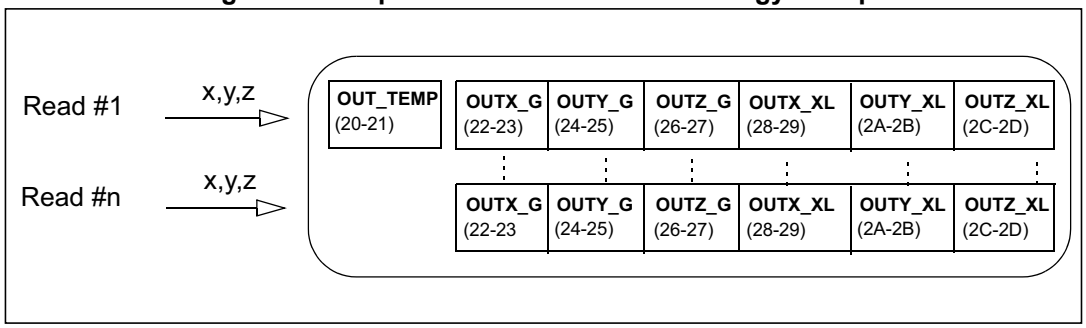
When only the accelerometer is activated and the gyroscope is in power down, starting from *OUT_TEMP_L (20h), OUT_TEMP_H (21h)* multiple reads can be performed. Once the read reaches *OUTZ_XL (2Ch - 2Dh)*, the system automatically restarts from *OUTX_XL (28h - 29h)* (see *Figure 5*).

Figure 5. Multiple reads: accelerometer only



When both accelerometer and gyroscope sensors are activated at the same ODR, starting from *OUT_TEMP_L (20h), OUT_TEMP_H (21h)* multiple reads can be performed. Once the read reaches *OUTZ_XL (2Ch - 2Dh)* the system automatically restarts from *OUTX_G (22h - 23h)* (see *Figure 6*).

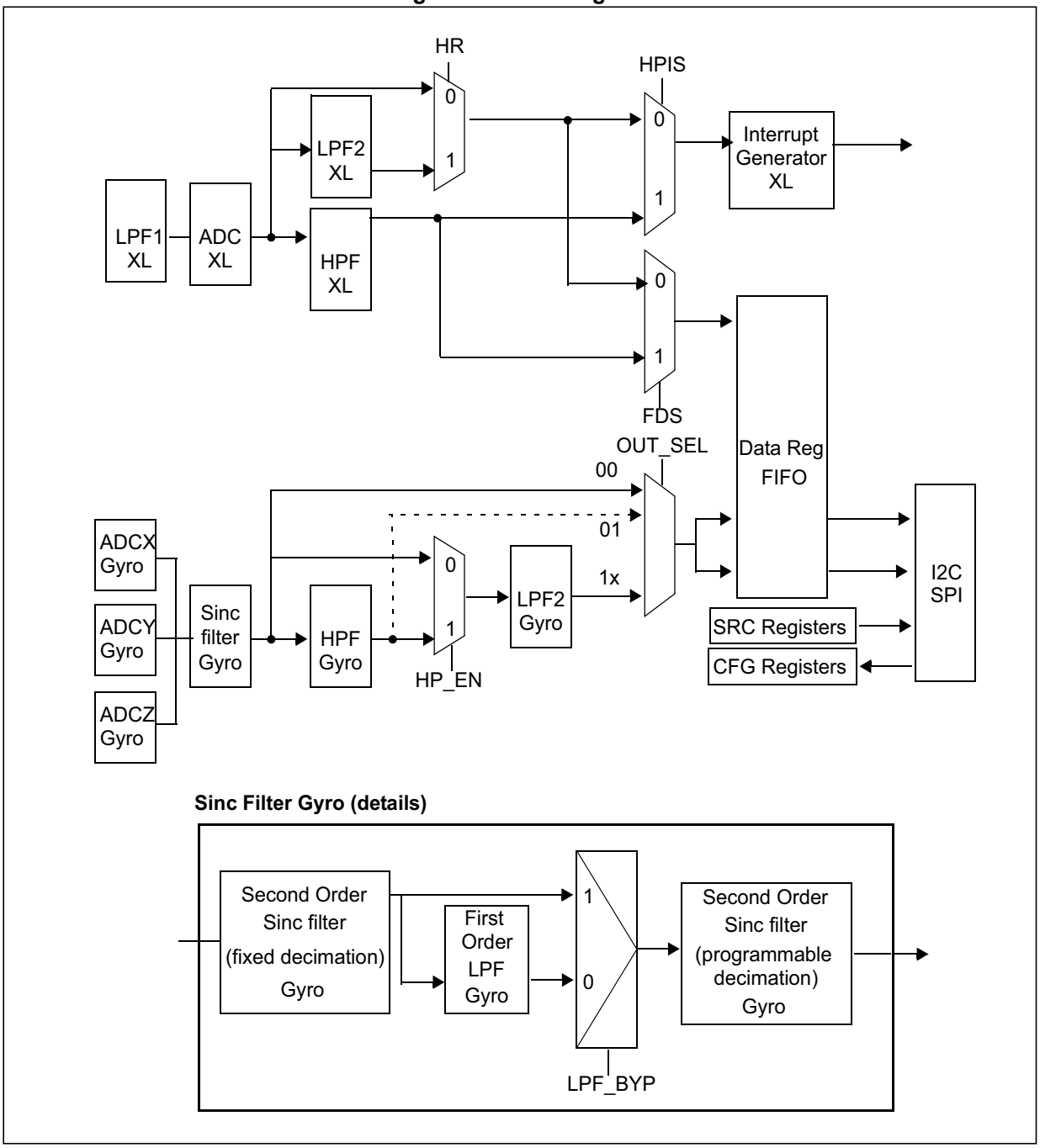
Figure 6. Multiple reads: accelerometer and gyroscope



3 Digital main block

3.1 Block diagram

Figure 7. Block diagram



3.2 FIFO

The ASM330LXH embeds 32 slots of 16-bit data FIFO for each of the gyroscope's three output channels, yaw, pitch and roll, and 16-bit data FIFO for each of the accelerometer's three output channels, X, Y and Z. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO. This buffer can work according to six different modes: Bypass mode, FIFO mode, Stream mode, Dynamic Stream mode, Stream-to-FIFO mode and Bypass-to-Stream. Each mode is selected by the FMODE [2:0] bits in the *FIFO_CTRL (1Ah)* register. Programmable FIFO threshold status, FIFO overrun events and the number of unread samples stored are available in the *FIFO_SRC (1Eh)* register.

FIFO_SRC(FTH) goes to '1' when the number of unread samples (FIFO_SRC(FSS5:0)) is greater than or equal to FTH [4:0] in *FIFO_CTRL (1Ah)*. If FIFO_CTRL(FTH4:0) is equal to 0, FIFO_SRC(FTH) goes to '0'.

FIFO_SRC(OVRN) is equal to '1' if a FIFO slot is overwritten.

FIFO_SRC(FSS5:0) contains stored data levels of unread samples; when FSS [5:0] is equal to '000000' FIFO is empty, when FSS [5:0] is equal to '100000' FIFO is full and the unread samples are 32.

The FIFO feature is enabled by writing '1' in CTRL5_C (FIFO_EN).

To guarantee the switching into and out of FIFO mode, discard the first sample acquired.

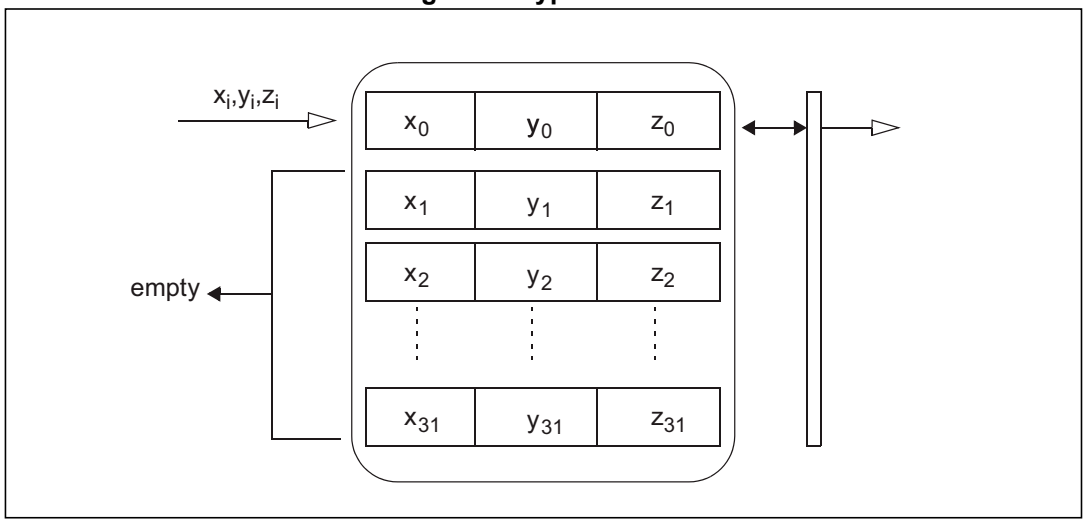
3.2.1 Bypass mode

In Bypass mode (FIFO_CTRL(FMODE2:0) = 000), the FIFO is not operational and it remains empty.

Bypass mode is also used to reset the FIFO when in FIFO mode.

As described in the next figure, for each channel only the first address is used. When new data is available, the older data is overwritten.

Figure 8. Bypass mode



3.2.2 FIFO mode

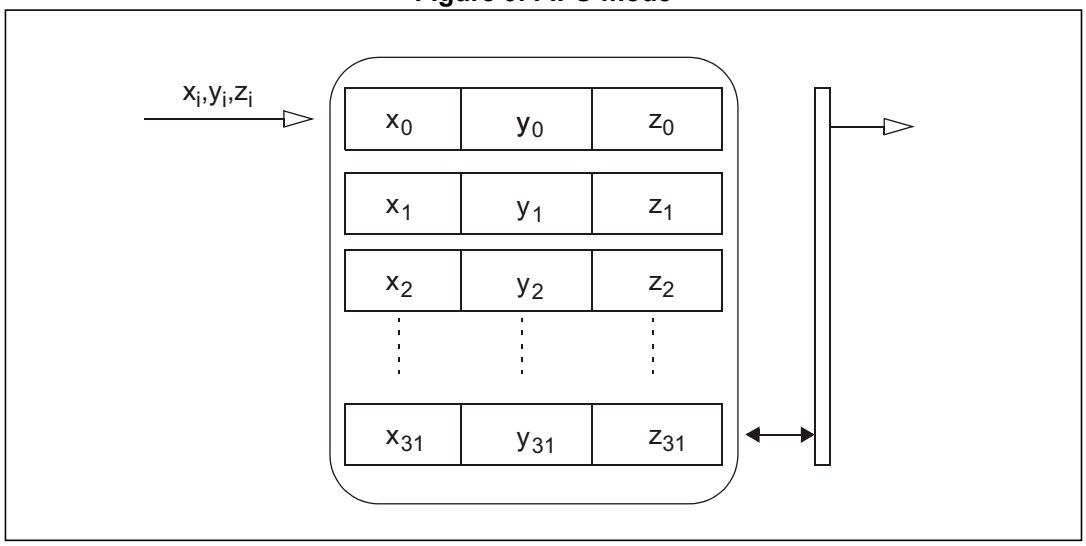
In FIFO mode (FIFO_CTRL(FMODE2:0) = 001) data from the output channels are stored in the FIFO until it is overwritten.

To reset FIFO content, Bypass mode must be written in FIFO_CTRL(FMODE2:0), setting these bits to '000' value. After this reset command it is possible to restart FIFO mode by writing the value '001' in FIFO_CTRL(FMODE2:0).

The FIFO buffer can memorize up to 32 levels of data but the depth of the FIFO can be resized by setting the CTRL4_C(STOP_ON_FTH) bit. If the STOP_ON_FTH bit is set to '1', FIFO depth is limited to FIFO_CTRL(FTH4:0) + 1 data.

A FIFO threshold interrupt can be enabled (INT_OVR bit in *INT_CTRL (0Dh)*) in order to be raised when the FIFO is filled to the level specified by the FTH4:0 bits of *FIFO_CTRL (1Ah)*. When a FIFO threshold interrupt occurs, the first data has been overwritten and the FIFO stops collecting data from the input channels.

Figure 9. FIFO mode



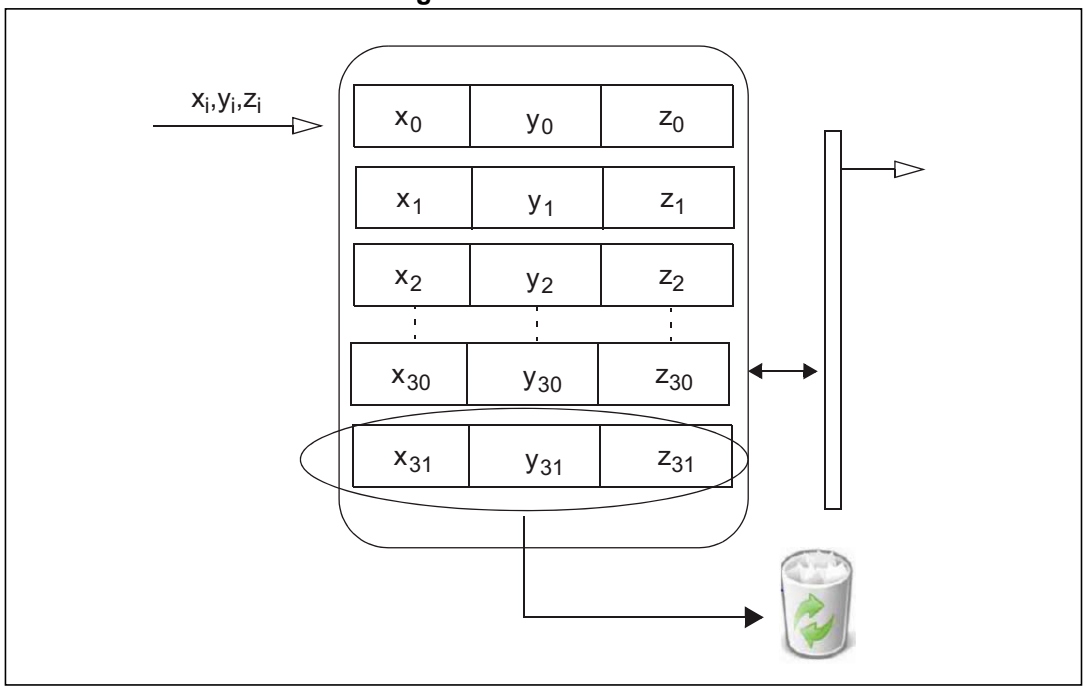
3.2.3 Stream mode

Stream mode (FIFO_CTRL(FMODE2:0) = 010) provides continuous FIFO update: as new data arrives, the older is discarded.

Once the whole FIFO has been read, the last data read remains in the FIFO and hence once a new sample is acquired, the FIFO_SRC(FSS5:0) value rises from 0 to 2.

An overrun interrupt can be enabled, INT_CTRL(INT1_OVR) = '1', in order to inform when the FIFO is full and eventually read its content all at once. If an overrun occurs, the oldest sample in FIFO is overwritten, so if the FIFO was empty, the lost sample has already been read.

Figure 10. Stream mode



In the latter case reading all FIFO content before an overrun interrupt has occurred, the first data read is equal to the last already read in the previous burst, so the number of new data available in FIFO depends on the previous reading.

3.2.4 Dynamic Stream mode

In Dynamic Stream mode (FIFO_CTRL(FMODE2:0) = 110) after emptying the FIFO, the first new sample that arrives becomes the first to be read in a subsequent read burst. In this way the number of new data available in FIFO does not depend on the previous reading.

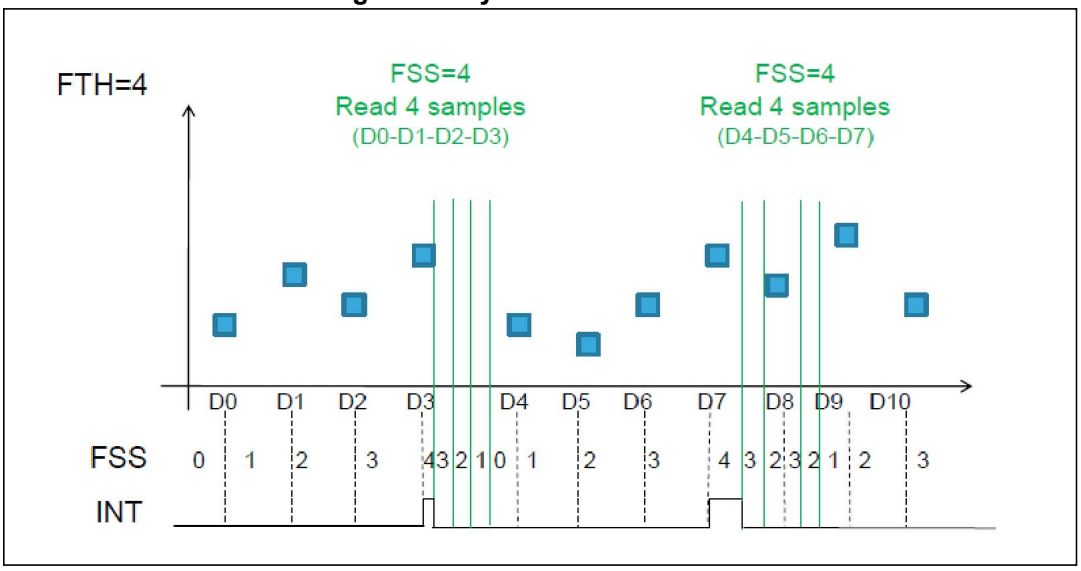
In Dynamic Stream mode FIFO_SRC(FSS5:0) is the number of new X, Y and Z samples available in the FIFO buffer.

Stream Mode is intended to be used to read all 32 samples of FIFO within an ODR after receiving an overrun signal.

Dynamic Stream is intended to be used to read FIFO_SRC(FSS5:0) samples when it is not possible to guarantee reading data within an ODR.

Also, a FIFO threshold interrupt on the INT pad through INT_CTRL(INT_FTH) can be enabled in order to read data from the FIFO and leave free memory slots for incoming data.

Figure 11. Dynamic Stream mode



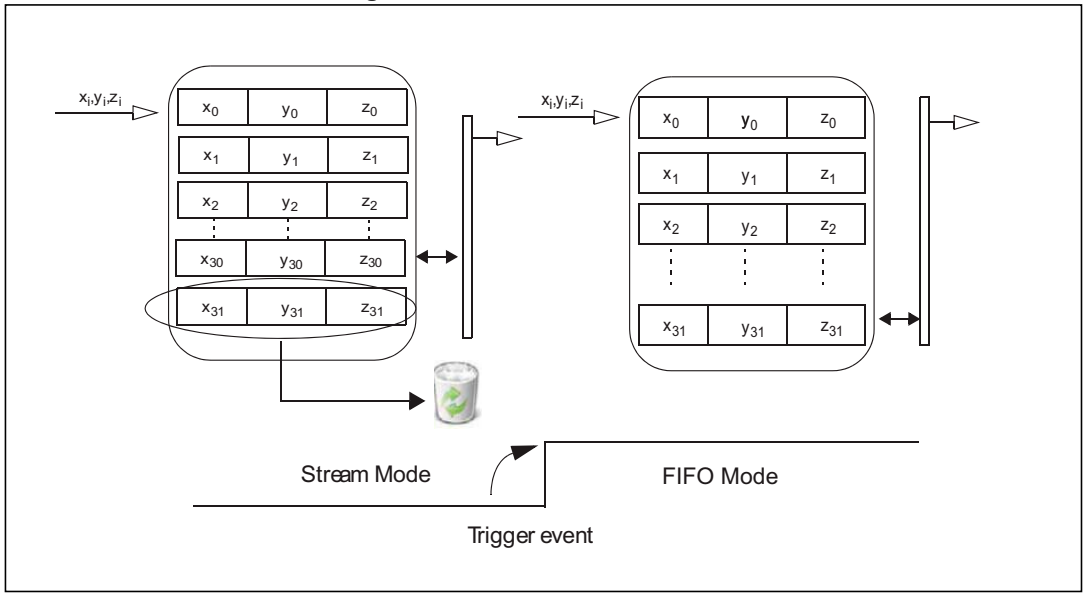
3.2.5 Stream-to-FIFO mode

In Stream-to-FIFO mode (FIFO_CTRL(FMODE2:0) = 011), FIFO behavior changes according to the INT_SRC_XL(IA_XL) bit. When the INT_SRC_XL(IA_XL) bit is equal to '1', FIFO operates in FIFO mode, when the INT_SRC_XL(IA_XL) bit is equal to '0' FIFO operates in Stream mode.

The interrupt generator should be set to the desired configuration by means of INT_CFG_XL, INT_THS_X_XL, INT_THS_Y_XL, INT_THS_Z_XL.

The CTRL10_C(LIR_XL) bit should be set to '1' in order to have latched interrupt.

Figure 12. Stream-to-FIFO mode



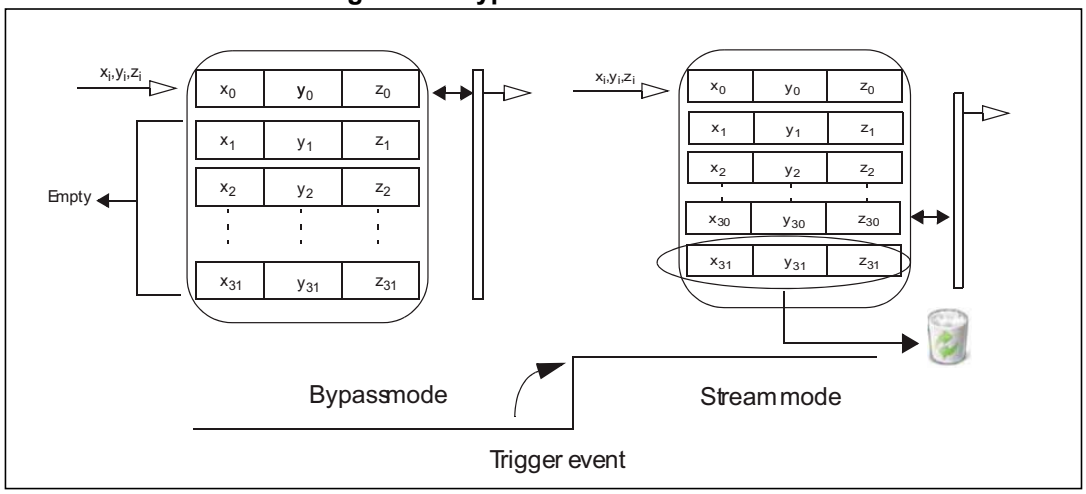
3.2.6 Bypass-to-Stream mode

In Bypass-to-Stream mode (FIFO_CTRL(FMODE2:0) = '100'), data measurement storage inside FIFO operates in Stream mode when INT_SRC_XL(IA_XL) is equal to '1', otherwise FIFO content is reset (Bypass mode).

The interrupt generator should be set to the desired configuration by means of INT_CFG_XL, INT_THS_X_XL, INT_THS_Y_XL, INT_THS_Z_XL.

The CTRL10_C(LIR_XL) bit should be set to '1' in order to have latched interrupt.

Figure 13. Bypass-to-Stream mode



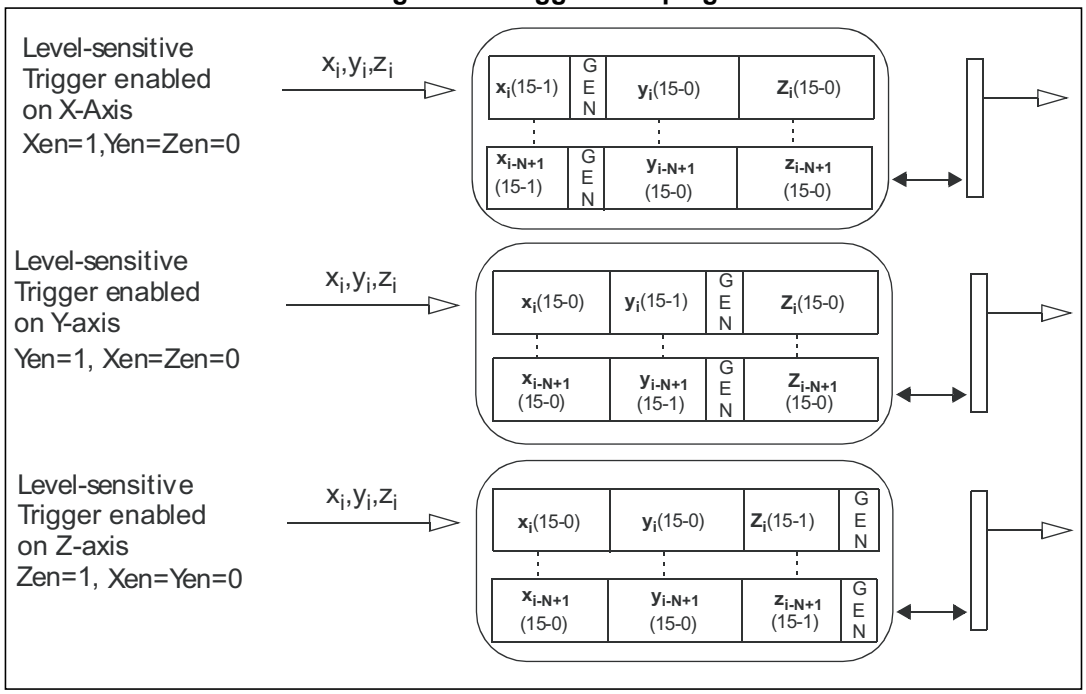
3.3 Level-sensitive/edge-sensitive/impulse-sensitive data enable

The ASM330LXH allows external trigger level recognition by enabling the EXTREn, LVLen and IMPen bits in *CTRL6_G (15h)* only when both the accelerometer and gyroscope are working. Three different modes can be used: level-, edge- or impulse-sensitive trigger.

Table 9. Trigger stamping mode

LVLen	EXTREn	IMPen	Trigger stamping mode
1	0	0	Level-sensitive trigger
0	1	0	Edge-sensitive trigger
1	0	1	Impulse-sensitive trigger

Figure 14. Trigger stamping



3.3.1 Level-sensitive trigger stamping

A level sensitive trigger can be enabled by setting the LVLen bit to '1' in CTRL6_G (15h) while the EXTREn bit in CTRL6_G (15h) and the IMPen bit in CTRL6_G (15h) have to be set to '0'.

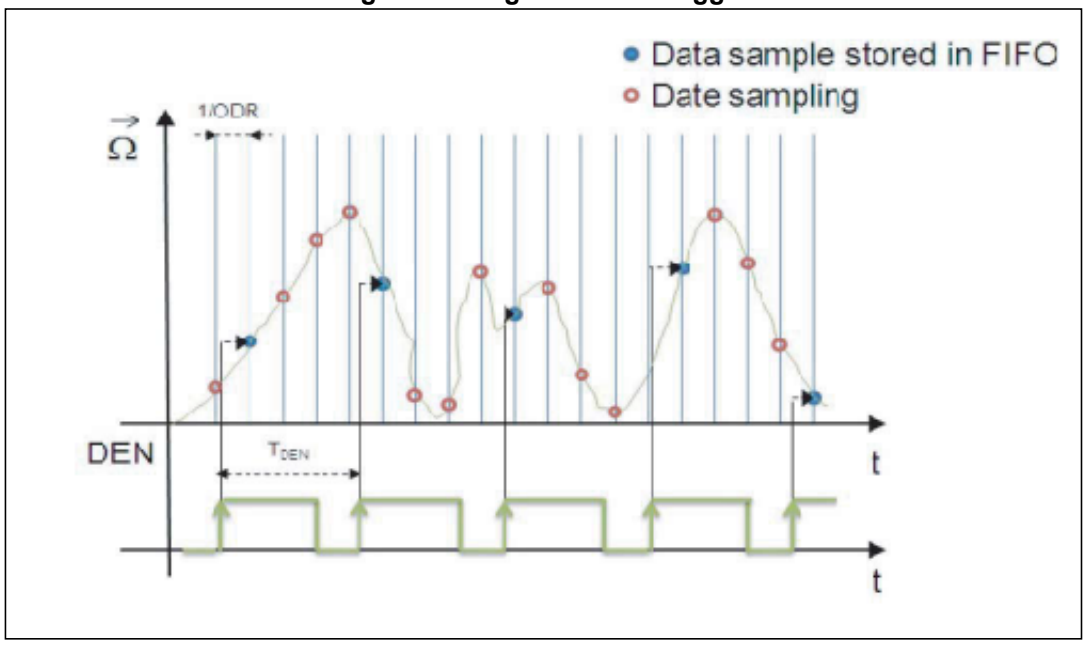
Once enabled, the G_EN level replaces the LSB of the X, Y or Z axes, configurable through the Xen, Yen, Zen bits in CTRL10_C (19h). Data is stored inside the FIFO with the internally-selected ODR.

3.3.2 Edge-sensitive trigger

An edge-sensitive trigger can be enabled by setting the EXTRen bit to '1' in CTRL6_G (15h) while the LVLen bit in CTRL6_G (15h) and the IMPen bit in CTRL6_G (15h) have to be set to '0'.

Once enabled, FIFO is filled with the pitch, roll and yaw data on the rising edge of the G_EN input signal. When the ODR selected is 800 Hz, the maximum G_EN sampling frequency is f_{G_EN} =1/T_{G_EN} = 400 Hz.

Figure 15. Edge-sensitive trigger



3.3.3 Impulse-sensitive trigger

An impulse-sensitive trigger can be enabled by setting the LVLen bit to '1' in CTRL6_G (15h) and the IMPen bit in CTRL6_G (15h) while the EXTRen bit in CTRL6_G (15h) has to be set to '0'.

If the duration of the G_EN pulse is shorter than the selected ODR, the impulse-sensitive trigger functionality has to be enabled.

4 Digital interfaces

The registers embedded inside the ASM330LXH may be accessed through both the I^2C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode and it is compliant with SPI transfer mode 3 and SPI transfer mode 0.

The serial interfaces are mapped onto the same pins. To select/exploit the I^2C interface, the CS line must be tied high (i.e connected to Vdd_IO).

Table 10. Serial interface pin description

Pin name	Pin description
CS	SPI enable I^2C/SPI mode selection (1: I^2C mode; 0: SPI enabled)
SCL/SPC	I^2C Serial Clock (SCL) SPI Serial Port Clock (SPC)
SDA/SDI/SDO	I^2C Serial Data (SDA) SPI Serial Data Input (SDI) 3-wire Interface Serial Data Output (SDO)
SDO/SA0	SPI Serial Data Output (SDO) I^2C less significant bit of the device address

4.1 I^2C serial interface

The ASM330LXH I^2C is a bus slave. The I^2C is employed to write the data to the registers, whose content can also be read back.

The relevant I^2C terminology is provided in the table below.

Table 11. I^2C terminology

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the serial clock line (SCL) and the Serial DAta line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines must be connected to Vdd_IO through an external pull-up resistor. When the bus is free, both the lines are high.

The I^2C interface is implemented with fast mode (400 kHz) I^2C standards as well as with the standard mode.

In order to disable the I^2C block, the I2C_disable bit of CTRL4_C must be set to 1.

4.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH-to-LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The Slave ADdress (SAD) associated to the ASM330LXH is 110101xb. The SDO/SA0 pin can be used to modify the less significant bit of the device address. If the SDO/SA0 pin is connected to the voltage supply, LSb is ‘1’ (address 1101011b), else if the SDO/SA0 pin is connected to ground, LSb is ‘0’ (address 1101010b). This solution permits to connect and address two different inertial modules to the same I²C bus.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the ASM330LXH behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted. The increment of the address is configured by CTRL3_C (IF_ADD_INC).

The slave address is completed with a Read/Write bit. If the bit is ‘1’ (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is ’0’ (Write) the master will transmit to the slave with direction unchanged. *Table 12* explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Table 12. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	110101	0	1	11010101 (D5h)
Write	110101	0	0	11010100 (D4h)
Read	110101	1	1	11010111 (D7h)
Write	110101	1	0	11010110 (D6h)

Table 13. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 14. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 15. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 16. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left HIGH by the slave. The master can then abort the transfer. A LOW-to-HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

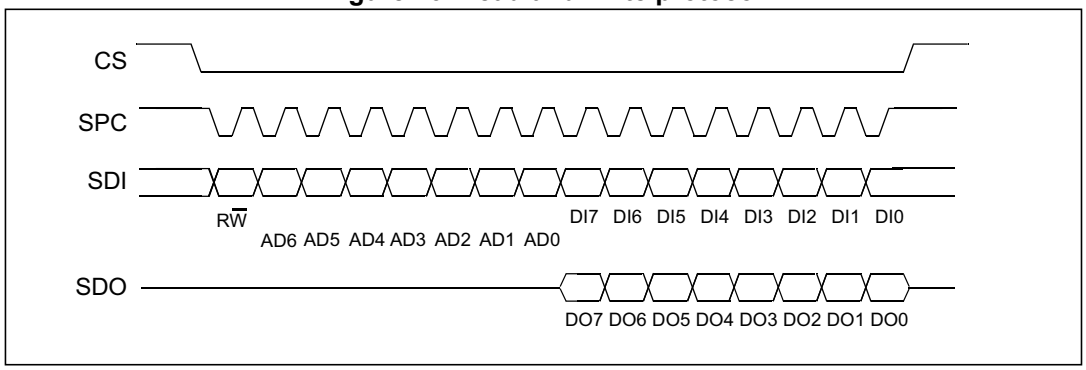
In the presented communication format MAK is Master acknowledge and NMAK is No Master Acknowledge.

4.2 SPI bus interface

The ASM330LXH SPI is a bus slave. The SPI allows writing to and reading from the registers of the device. It is compliant with SPI transfer mode 3 and SPI transfer mode 0.

The serial interface interacts with the outside world with 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 16. Read and write protocol



CS is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS**.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip will drive **SDO** at the start of bit 8.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

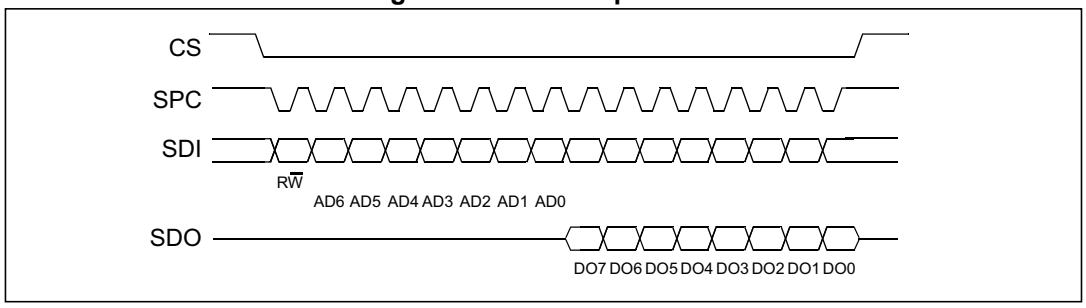
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods will be added. When the CTRL3_C (IF_ADD_INC) bit is '0' the address used to read/write data remains the same for every block. When the CTRL3_C (IF_ADD_INC) bit is '1' the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

4.2.1 SPI read

Figure 17. SPI read protocol



The SPI read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

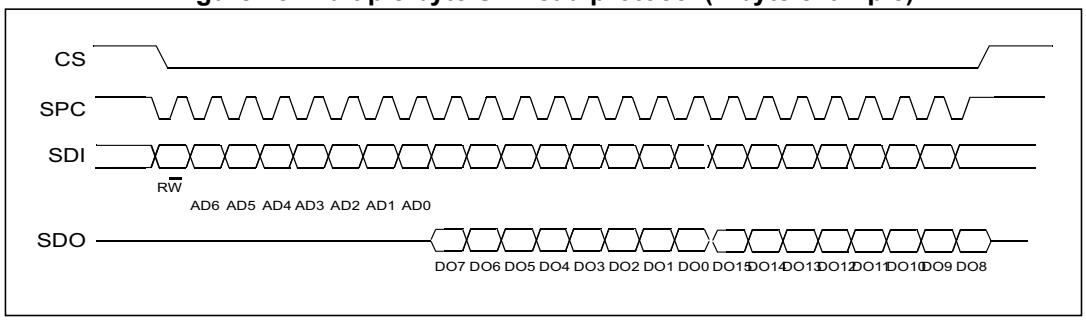
bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

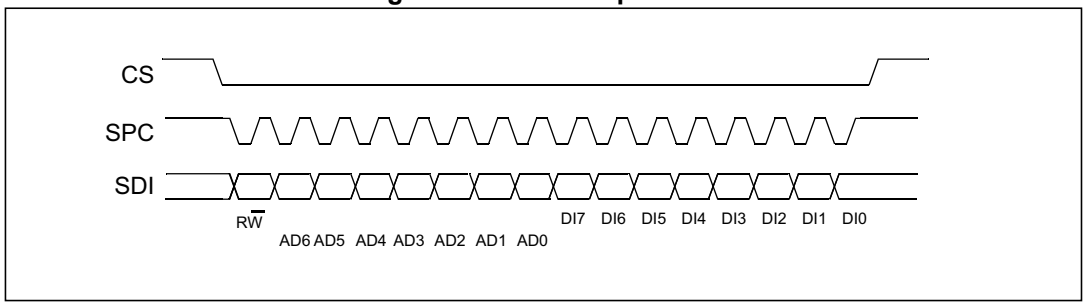
bit 16-... : data DO(...-8). Further data in multiple byte reads.

Figure 18. Multiple byte SPI read protocol (2-byte example)



4.2.2 SPI write

Figure 19. SPI write protocol



The SPI write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

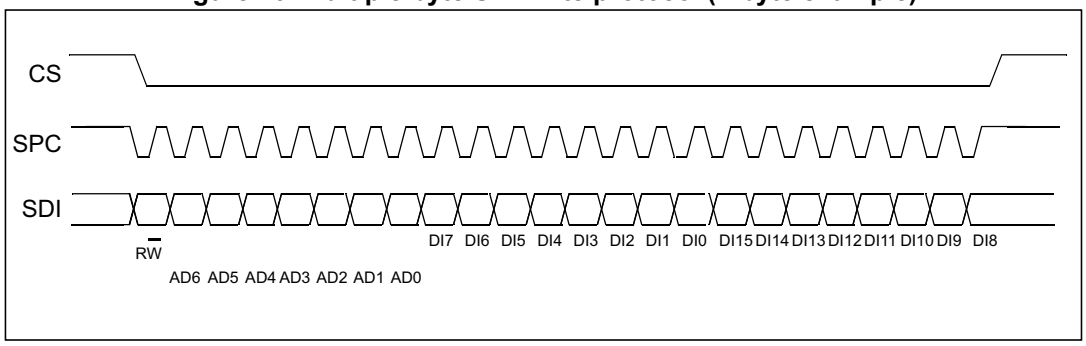
bit 0: WRITE bit. The value is 0.

bit 1 -7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writes.

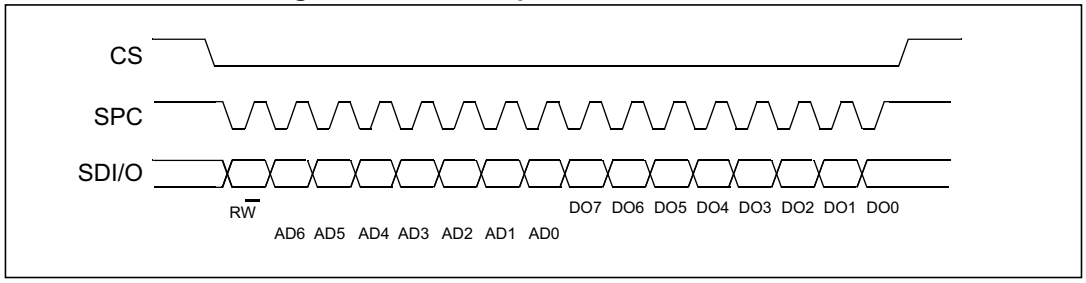
Figure 20. Multiple byte SPI write protocol (2-byte example)



4.2.3 SPI read in 3-wire mode

3-wire mode is entered by setting the CTRL3_C (SIM) bit equal to ‘1’ (SPI serial interface mode selection).

Figure 21. SPI read protocol in 3-wire mode



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

A multiple read command is also available in 3-wire mode.

5 Register mapping

The tables given below provides a list of the 8/16 bit registers embedded in the device and the corresponding addresses.

Table 17. Register map

Name	Type	Register address		Default	Comment
		Hex	Binary		
RESERVED	-	00	00000000	-	Reserved
RESERVED	-	01	00000001	-	Reserved
RESERVED	-	02	00000010	-	Reserved
RESERVED	-	03	00000011	-	Reserved
ACT_THS	r/w	04	00000100	-	
ACT_DUR	r/w	05	00000101	00000000	
INT_CFG_XL	r/w	06	00000110	00000000	
INT_THS_X_XL	r/w	07	00000111	00000000	
INT_THS_Y_XL	r/w	08	00001000	00000000	
INT_THS_Z_XL	r/w	09	00001001	00000000	
INT_DUR_XL	r/w	0A	00001010	00000000	
ORIENT_CFG_G	r/w	0B	00001011	00000000	
REFERENCE_G	r/w	0C	00001100	00000000	
INT_CTRL	r/w	0D	00001101	00000000	INT pin control
RESERVED	r/w	0E	00001110	00000000	Reserved
WHO_AM_I	r	0F	00001111	01100001	Who I am ID
CTRL1_XL	r/w	10	00010000	00000000	
CTRL2_G	r/w	11	00010001	00000000	
CTRL3_C	r/w	12	00010010	00000100	
CTRL4_C	r/w	13	00010011	00000000	
CTRL5_C	r/w	14	00010100	00000000	
CTRL6_G	r/w	15	00010101	00000000	
CTRL7_G	r/w	16	00010110	00000000	
CTRL8_XL	r/w	17	00010111	00000000	
CTRL9_XL	r/w	18	00011000	00111000	
CTRL10_C	r/w	19	00011001	00111000	
FIFO_CTRL	r/w	1A	00011010	00000000	
RESERVED	-	1B	00011011	-	Reserved
RESERVED	-	1C	00011100	-	Reserved

Table 17. Register map (continued)

Name	Type	Register address		Default	Comment
		Hex	Binary		
INT_SRC_XL	r	1D	00011101	output	
FIFO_SRC	r	1E	00011110	output	
STATUS_REG	r	1F	00011111	output	Status data register
OUT_TEMP_L	r	20	00100000	output	Temperature sensor data register
OUT_TEMP_H	r	21	00100001	output	
OUTX_L_G	r	22	00100010	output	Gyroscope output registers
OUTX_H_G	r	23	00100011	output	
OUTY_L_G	r	24	00100100	output	
OUTY_H_G	r	25	00100101	output	
OUTZ_L_G	r	26	00100110	output	
OUTZ_H_G	r	27	00100111	output	
OUTX_L_XL	r	28	00101000	output	Accelerometer output registers
OUTX_H_XL	r	29	00101001	output	
OUTY_L_XL	r	2A	00101010	output	
OUTY_H_XL	r	2B	00101011	output	
OUTZ_L_XL	r	2C	00101100	output	
OUTZ_H_XL	r	2D	00101101	output	
RESERVED	r	2E - 2F	-	-	Reserved
RESERVED	-	30	00110000	-	Reserved
RESERVED	-	31	00110001	-	Reserved
RESERVED	-	32	00110010	-	Reserved
LPF_BYP_REG	r/w	33	00110011	00000000	
RESERVED	-	34	00110100	-	Reserved
RESERVED	-	35	00110101	-	Reserved
RESERVED	-	36	00110110	-	Reserved
RESERVED	-	37	00110111	-	Reserved
RESERVED	-	38-7F	-	-	Reserved

Registers marked as *Reserved* must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

6 Register description

The device contains a set of registers which are used to control its behavior and to retrieve linear acceleration, angular rate and temperature data. The register addresses, made up of 7 bits, are used to identify them and to write the data through the serial interface.

6.1 ACT_THS (04h)

Activity threshold register (r/w).

Table 18. ACT_THS register

SLEEP_ON _INACT_EN	ACT_THS 6	ACT_THS 5	ACT_THS 4	ACT_THS 3	ACT_THS 2	ACT_TH S1	ACT_THS 0

Table 19. ACT_THS register description

SLEEP_ON_ INACT_EN	Gyroscope operating mode during inactivity. Default value: 0. (0: Gyroscope in power down; 1: Gyroscope in sleep mode)
ACT_THS [6:0]	Inactivity threshold. Default value: 000 0000.

6.2 ACT_DUR (05h)

Inactivity duration register (r/w).

Table 20. ACT_DUR register

ACT_DUR 7	ACT_DUR 6	ACT_DUR 5	ACT_DUR 4	ACT_DUR 3	ACT_DUR 2	ACT_DUR 1	ACT_DUR 0

Table 21. ACT_DUR register description

ACT_DUR [7:0]	Inactivity duration. Default value: 0000 0000.

6.3 INT_CFG_XL (06h)

Linear acceleration sensor interrupt generator configuration register (r/w).

Table 22. INT_CFG_XL register

AOI_XL	6D	ZHIE_XL	ZLIE_XL	YHIE_XL	YLIE_XL	XHIE_XL	XLIE_XL

Table 23. INT_CFG1_XL register description

AOI_XL	AND/OR combination of accelerometer's interrupt events. Default value: 0. (0: OR combination; 1: AND combination)
6D	6 direction detection function for interrupt. Default value: 0. (0: disabled; 1: enabled)
ZHIE_XL	Enable interrupt generation on accelerometer's Z-axis high event. Default value: 0. (0: disable interrupt request; 1: interrupt request on measured acceleration value higher than preset threshold)
ZLIE_XL	Enable interrupt generation on accelerometer's Z-axis low event. Default value: 0. (0: disable interrupt request; 1: interrupt request on measured acceleration value higher than preset threshold)
YHIE_XL	Enable interrupt generation on accelerometer's Y-axis high event. Default value: 0. (0: disable interrupt request; 1: interrupt request on measured acceleration value higher than preset threshold)
YLIE_XL	Enable interrupt generation on accelerometer's Y-axis low event. Default value: 0. (0: disable interrupt request; 1: interrupt request on measured acceleration value higher than preset threshold)
XHIE_XL	Enable interrupt generation on accelerometer's X-axis high event. Default value: 0. (0: disable interrupt request; 1: interrupt request on measured acceleration value higher than preset threshold)
XLIE_XL	Enable interrupt generation on accelerometer's X-axis low event. Default value: 0. (0: disable interrupt request; 1: interrupt request on measured acceleration value higher than preset threshold)

6.4 INT_THS_X_XL (07h)

Linear acceleration sensor interrupt threshold register (r/w).

Table 24. INT_THS_X_XL register

THS_XL_X7	THS_XL_X6	THS_XL_X5	THS_XL_X4	THS_XL_X3	THS_XL_X2	THS_XL_X1	THS_XL_X0

Table 25. INT_THS_X_XL register description

THS_XL_X [7:0]	X-axis interrupt thresholds. Default value: 0000 0000.

6.5 INT_THS_Y_XL (08h)

Linear acceleration sensor interrupt threshold register (r/w).

Table 26. INT_THS_Y_XL register

THS_XL_Y7	THS_XL_Y6	THS_XL_Y5	THS_XL_Y4	THS_XL_Y3	THS_XL_Y2	THS_XL_Y1	THS_XL_Y0

Table 27. INT_THS_Y_XL register description

THS_XL_Y [7:0]	Y-axis interrupt thresholds. Default value: 0000 0000.

6.6 INT_THS_Z_XL (09h)

Linear acceleration sensor interrupt threshold register (r/w).

Table 28. INT_THS_Z_XL register

THS_XL_Z7	THS_XL_Z6	THS_XL_Z5	THS_XL_Z4	THS_XL_Z3	THS_XL_Z2	THS_XL_Z1	THS_XL_Z0

Table 29. INT_THS_Z_XL register description

THS_XL_Z [7:0]	Z-axis interrupt thresholds. Default value: 0000 0000.

6.7 INT_DUR_XL (0Ah)

Linear acceleration sensor interrupt duration register (r/w).

Table 30. INT_DUR_XL register

WAIT_XL	DUR_XL6	DUR_XL5	DUR_XL4	DUR_XL3	DUR_XL2	DUR_XL1	DUR_XL0

Table 31. INT_DUR_XL register description

WAIT_XL	Wait function enable on duration counter. Default value: 0. (0: wait function off; 1: wait for DUR_XL [6:0] samples before exiting interrupt)
DUR_XL [6:0]	Enter/exit interrupt duration value. Default value: 000 0000.

6.8 ORIENT_CFG_G (0Bh)

Angular rate sensor sign and orientation register (r/w).

Table 32. ORIENT_CFG_G register

0(1)	DRDY_mask_bit_CFG2	SignX_G	SignY_G	SignZ_G	Orient_2	Orient_1	Orient_0

1. This bit must be set to ‘0’ for the correct operation of the device.

Table 33. ORIENT_CFG_G register description

DRDY_mask_bit _CFG2	Configuration 2[(1)] data available enable bit. Default value: 0. (0: DA timer disabled; 1: DA timer enabled)
SignX_G	Pitch axis (X) angular rate sign. Default value: 0. (0: positive sign; 1: negative sign)
SignY_G	Roll axis (Y) angular rate sign. Default value: 0. (0: positive sign; 1: negative sign)
SignZ_G	Pitch axis (Z) angular rate sign. Default value: 0. (0: positive sign; 1: negative sign)
Orient [2:0]	Directional user-orientation selection. Default value: 000.

1. In Configuration 2, switching to Combo mode, gyroscope data is used to discriminate the condition:
   - "7FFF": Accel-only mode
   - "7FFE": Combo mode, driving setting phase on-going
   - "7FFD": Combo mode, driving setting phase completed.

   Switching to accelerometer-only, data are collected in FIFO after filter setting.

6.9 REFERENCE_G (0Ch)

Angular rate sensor reference value register for digital high-pass filter (r/w).

Table 34. REFERENCE_G register

REF7_G	REF6_G	REF5_G	REF4_G	REF3_G	REF2_G	REF1_G	REF0_G

Table 35. REFERENCE_G register description

REF[7:0]_G	Reference value for gyroscope's digital high-pass filter. Default value: 0000 0000.

6.10 INT_CTRL (0Dh)

INT pad control register (r/w).

Table 36. INT1_CTRL register

0	INT_IG _XL	INT_FSS5	INT_OVR	INT_FTH	INT_Boot	INT_ DRDY_G	INT_ DRDY_XL

Table 37. INT_CTRL register description

INT_ IG_XL	Accelerometer interrupt generator on INT pad. Default value: 0. (0: disabled; 1: enabled)
INT_ FSS5	FSS5 interrupt enable on INT pad. Default value: 0. (0: disabled; 1: enabled)
INT_OVR	Overrun Interrupt on INT pad. Default value: 0. (0: disabled; 1: enabled)
INT_FTH	FIFO threshold interrupt on INT pad. Default value: 0. (0: disabled; 1: enabled)
INT_ Boot	Boot status available on INT pad. Default value: 0. (0: disabled; 1: enabled)
INT_DRDY_G	Gyroscope data ready on INT pad. Default value: 0. (0: disabled; 1: enabled)
INT_DRDY_XL	Accelerometer data ready on INT pad. Default value: 0. (0: disabled; 1: enabled)

6.11 WHO_AM_I (0Fh)

Who_AM_I register (r). This register is a read-only register. Its value is fixed at 61h.

Table 38. WHO_AM_I register

0	1	1	0	0	0	0	1

6.12 CTRL1_XL (10h)

Linear acceleration sensor Control Register 1 (r/w).

Table 39. CTRL1_XL register

ODR_XL2	ODR_XL1	ODR_XL0	FS1_XL	FS0_XL	BW_SCAL_ODR	BW_XL1	BW_XL0

Table 40. CTRL1_XL register description

ODR_XL [2:0]	Output data rate and power mode selection. Default value: 000 (see *Table 41*).
FS_XL [1:0]	Accelerometer full-scale selection. Default value: 00. (00: ±2 *g*; 01: ±16 *g*; 10: ±4 *g*; 11: ±8 *g*)
BW_SCAL_ODR	Bandwidth determination selection. Default value: 0. (0: bandwidth determined by ODR selection as in *Table 42* 1: bandwidth selected according to BW_XL[1:0] selection)
BW_XL [1:0]	Anti-aliasing filter bandwidth selection. Default value: 00. 00: 380 Hz; 01: 190 Hz; 10: 95 Hz; 11: 47.5 Hz.

ODR_XL [2:0] is used to set power mode and ODR selection. The following table *Table 41: ODR register setting* indicates all available frequencies when only the accelerometer is activated.

Table 41. ODR register setting

ODR_XL2	ODR_XL1	ODR_XL0	ODR selection [Hz]
0	0	0	Power down
0	0	1	12.5 Hz
0	1	0	50 Hz
0	1	1	100 Hz
1	0	0	200 Hz
1	0	1	400 Hz
1	1	0	800 Hz
1	1	1	n.a.

When BW_SCAL_ODR is set to ‘0’, the bandwidth is determined by the ODR selection. *Table 42: BW and ODR (normal mode)* indicates the bandwidth for all available frequencies.

Table 42. BW and ODR (normal mode)

BW	ODR selection [Hz]
380	800 Hz, 50 Hz, 12.5 Hz
190	400 Hz
95	200 Hz
47.5	100 Hz

6.13 CTRL2_G (11h)

Angular rate sensor Control Register 2 (r/w).

Table 43. CTRL2_G register

ODR_G2	ODR_G1	ODR_G0	FS_G1	FS_G0	FS_125	BW_G1	BW_G0

Table 44. CTRL2_G register description

ODR_G [2:0]	Gyroscope output data rate selection. Default value: 000. (Refer to *Table 45* and *Table 46*)
FS_G [1:0]	Gyroscope full-scale selection. Default value: 00. (00: 245 dps; 01: 500 dps; 10: 1000 dps; 11: 2000 dps)
FS_125	Gyroscope full scale at 125 dps. Default value: 0. (0: disabled; 1: enabled)
BW_G [1:0]	Gyroscope bandwidth selection. Default value: 00.

ODR_G [2:0] is used to set ODR selection when both the accelerometer and gyroscope are activated. BW_G [1:0] is used to set bandwidth selection.

Table 45 and *Table 46* indicate all available frequencies for combinations of the ODR_G / BW_G bits when both the accelerometer and gyroscope are activated.

For more details regarding signal processing scheme, please refer to *Figure 22*.

Table 45. ODR and BW configuration setting (no LPF2)

ODR_G2	ODR_G1	ODR_G0	ODR [Hz]	Cutoff [Hz](1) INT_THS_REG (LPF_BYP) = 1	Cutoff [Hz](1) INT_THS_REG (LPF_BYP) = 0
0	0	0	Power down	n.a.	n.a.
0	0	1	12.5	4	4
0	1	0	50	16	16
0	1	1	100	31	31
1	0	0	200	67	53
1	0	1	400	120	85
1	1	0	800	207	106
1	1	1	n.a.	n.a.	n.a.

1. Values in the table are indicative and can vary proportionally with the specific ODR value.

Table 46. ODR and BW configuration setting (after LPF2)

ODR_G [2:0]	BW_G [1:0]	ODR [Hz]	Cutoff [Hz](1)
000	00	Power down	n.a.
000	01	Power down	n.a.
000	10	Power down	n.a.
000	11	Power down	n.a.
001	00	12.5	n.a.
001	01	12.5	n.a.
001	10	12.5	n.a.
001	11	12.5	n.a.
010	00	50	16
010	01	50	16
010	10	50	16
010	11	50	16
011	00	100	12.5
011	01	100	26
011	10	100	26
011	11	100	26

Table 46. ODR and BW configuration setting (after LPF2) (continued)

ODR_G [2:0]	BW_G [1:0]	ODR [Hz]	Cutoff [Hz](1)
100	00	200	12.5
100	01	200	24
100	10	200	50
100	11	200	55
101	00	400	18
101	01	400	23.5
101	10	400	45
101	11	400	86
110	00	800	28
110	01	800	34
110	10	800	46
110	11	800	78
111	00	n.a.	n.a.
111	01	n.a.	n.a.
111	10	n.a.	n.a.
111	11	n.a.	n.a.

1. Values in the table are indicative and can vary proportionally with the specific ODR value.

6.14 CTRL3_C (12h)

Control register 3 (r/w).

Table 47. CTRL3_C register

BOOT	BDU	0(1)	PP_OD	SIM	IF_ADD_INC	BLE	SW_RESET

1. This bit must be set to ‘0’ for the correct operation of the device.

Table 48. CTRL3_C register description

BOOT	Reboot memory content. Default value: 0. (0: normal mode; 1: reboot memory content(1))
BDU	Block Data Update. Default value: 0. (0: continuous update; 1: output registers not updated until MSB and LSB have been read)
PP_OD	Push-Pull/Open-Drain selection on INT pad. Default value: 0. (0: push-pull mode; 1: open drain mode)
SIM	SPI Serial Interface Mode selection. Default value: 0. (0: 4-wire interface; 1: 3-wire interface).
IF_ADD_INC	Register address automatically incremented during a multiple byte access with a serial interface (I^2C or SPI). Default value: 1. (0: disabled; 1: enabled)

Table 48. CTRL3_C register description (continued)

BLE	Big/Little Endian Data Selection. Default value 0. (0: data LSB @ lower address; 1: data MSB @ lower address)
SW_RESET	Software Reset. Default value: 0. (0: normal mode; 1: reset device) This bit is cleared by hardware after next flash boot.

1. Boot request is executed as soon as internal oscillator is turned on. It is possible to set bit while in power-down mode, in this case it will be served at the next normal mode or sleep mode.

6.15 CTRL4_C (13h)

Control register 4 (r/w).

Table 49. CTRL4_C register

XL_LP_EN	SLEEP_G	0	FIFO_TEMP_EN	DRDY_mask_bit_CFG1	I2C_disable	FIFO_EN	STOP_ON_FTH

Table 50. CTRL4_C register description

XL_LP_EN	Accelerometer low-power/normal mode enable. Default value: 0. (0: normal mode; 1: low-power mode with ODR ≤ 100Hz)
SLEEP_G	Gyroscope sleep mode enable. Default value: 0. (0: disabled; 1: enabled)
FIFO_TEMP_EN	Temperature data storing in FIFO enable. Default value: 0. (0: temperature data not stored in FIFO; 1: temperature data stored in FIFO)
DRDY_mask_bit_CFG1	Configuration 1(1) Data Available Enable bit. Default value: 0. (0: DA timer disabled; 1: DA timer enabled)
I2C_disable	Disable I^2C interface. Default value: 0. (0: both I^2C and SPI enabled; 1: I^2C disabled, SPI only)
FIFO_EN	FIFO memory enable. Default value: 0. (0: disabled; 1: enabled)
STOP_ON_FTH	Enable FIFO threshold level use. Default value: 0. (0: FIFO depth is not limited; 1: FIFO depth is limited to threshold level)

1. In Configuration 1, switching to Combo mode, data are collected in FIFO only when both the accelerometer and gyroscope are set. Switching to accelerometer-only, data are collected in FIFO after filter setting.

6.16 CTRL5_C (14h)

Control Register 5 (r/w).

Table 51. CTRL5_C register

0(1)	0(1)	0(1)	0(1)	ST1_G	ST0_G	ST1_XL	ST0_XL

1. This bit must be set to '0' for the correct operation of the device.

Table 52. CTRL5_C register description

ST_G [1:0]	Angular rate sensor self-test enable. Default value: 00 (00: Self-test disabled; Other: refer to *Table 53*)
ST_XL [1:0]	Linear acceleration sensor self-test enable. Default value: 00 (00: Self-test disabled; Other: refer to *Table 54*)

Table 53. Angular rate sensor self-test mode selection

ST1_G	ST0_G	Self-test mode
0	0	Normal mode
0	1	Positive sign self-test
1	0	Not allowed
1	1	Negative sign self-test

Table 54. Linear acceleration sensor self-test mode selection

ST1_XL	ST0_XL	Self-test mode
0	0	Normal mode
0	1	Positive sign self-test
1	0	Negative sign self-test
1	1	Not allowed

6.17 CTRL6_G (15h)

Angular rate sensor Control Register 6 (r/w).

Table 55. CTRL6_G register

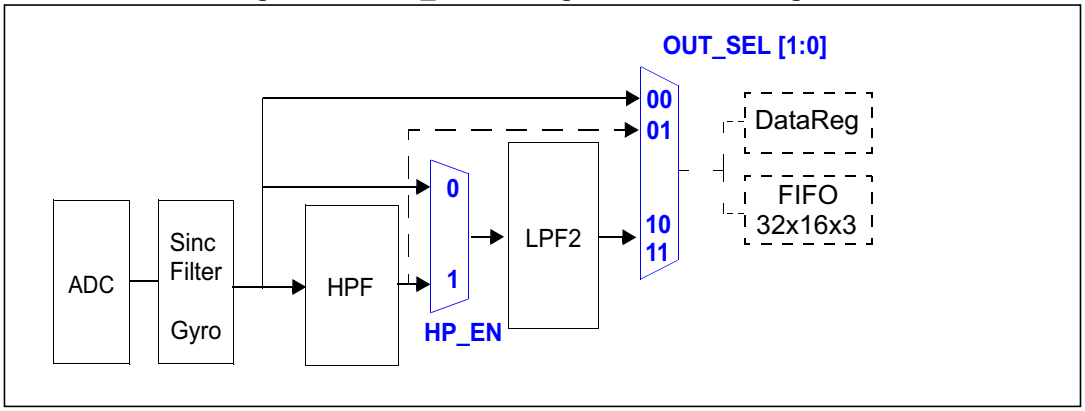
EXTRen	LVLen	IMPen	0(1)	0	0	OUT_SEL1	OUT_SEL0

1. This bit must be set to '0' for the correct operation of the device

Table 56. CTRL6_G register description

EXTRen	Data edge-sensitive trigger enable. Default value: 0. (0: external trigger disabled; 1: external trigger enabled)
LVLen	Data level-sensitive trigger Enable. Default value: 0. (0: level sensitive trigger disabled; 1: level sensitive trigger enabled)
IMPen	Level-sensitive latched enable. Default value: 0. (0: level sensitive latched disabled; 1: level sensitive latched enabled)
OUT_SEL [1:0]	Out selection configuration. Default value: 00 (Refer to *Figure 22*)

Figure 22. OUT_SEL configuration block diagram



6.18 CTRL7_G (16h)

Angular rate sensor Control Register 7 (r/w).

Table 57. CTRL7_G register

0(1)	HP_EN	HPM1_G	HPM0_G	HPCF3_G	HPCF2_G	HPCF1_G	HPCF0_G

1. This bit must be set to '0' for the correct operation of the device

Table 58. CTRL7_G register description

HP_EN	High-pass filter enable. Default value: 0. (0: HPF disabled; 1: HPF enabled, refer to *Figure 22*)
HPM[1:0]_G	Gyroscope high-pass filter mode selection. Default value: 00. Refer to *Table 59*.
HPCF[3:0]_G	Gyroscope high-pass filter cutoff frequency selection. Default value: 0000. Refer to *Table 60*.

Table 59. Gyroscope high-pass filter mode configuration

HPM1_G	HPM0_G	High-pass filter mode
0	0	Normal mode (reset by reading *REFERENCE_G (0Ch)* register)
0	1	Reference signal for filtering
1	0	Normal mode
1	1	Auto-reset on interrupt event

Table 60. Gyroscope high-pass filter cutoff frequency configuration [Hz](1)

HPCF_G [3:0]	ODR= 12.5 Hz	ODR= 50 Hz	ODR= 100 Hz	ODR= 200 Hz	ODR= 400 Hz	ODR= 800 Hz
0000	1	4	8	15	30	57
0001	0.5	2	4	8	15	30
0010	0.2	1	2	4	8	15
0011	0.1	0.5	1	2	4	8
0100	0.05	0.2	0.5	1	2	4
0101	0.02	0.1	0.2	0.5	1	2
0110	0.01	0.05	0.1	0.2	0.5	1
0111	0.005	0.02	0.05	0.1	0.2	0.5
1000	0.002	0.01	0.02	0.05	0.1	0.2
1001	0.001	0.005	0.01	0.02	0.05	0.1

1. Values in the table are indicative and can vary proportionally with the specific ODR value.

6.19 CTRL8_XL (17h)

Linear acceleration sensor Control Register 8 (r/w).

Table 61. CTRL8_XL register

HR	DCF_XL1	DCF_XL0	HPM_XL1	HPM_XL0	FDS	0	HPIS

Table 62. CTRL8_XL register description

HR	High-resolution mode for accelerometer enable. Default value: 0. (0: disabled; 1: enabled) Refer to *Table 63*
DCF_XL [1:0]	Accelerometer digital filter (high-pass and low-pass) cutoff frequency selection: the bandwidth of the high-pass filter depends on the selected ODR. Refer to *Table 63*
HPM_XL [1:0]	Accelerometer high-pass filter mode selection. Default value: 00. (00: Normal mode: 01: Reference signal for filtering; 10: Normal mode; 11: Auto-reset on interrupt event)

Table 62. CTRL8_XL register description (continued)

FDS	Filtered data selection. Default value: 0. (0: internal filter bypassed; 1: data from internal filter sent to output register and FIFO)
HPIS	High-pass filter enabled for accelerometer interrupt function on Interrupt 1. Default value: 0. (0: filter bypassed; 1: filter enabled)

Table 63. Low pass cut-off frequency in high-resolution mode (HR = 1)

CTRL8_XL (HR)	CTRL8_XL (DCF [1:0])	LP cutoff freq. [Hz]
1	00	ODR/50
1	01	ODR/100
1	10	ODR/9
1	11	ODR/400

6.20 CTRL9_XL (18h)

Linear acceleration sensor Control Register 9 (r/w).

Table 64. CTRL9_XL register

DEC_1	DEC_0	Zen_XL	Yen_XL	Xen_XL	0	0	0

Table 65. CTRL9_XL register description

DEC_ [1:0]	Decimation of acceleration data on OUT REG and FIFO. Default value: 00. (00: no decimation; 01: update every 2 samples; 10: update every 4 samples; 11: update every 8 samples)
Zen_XL	Accelerometer's Z-axis output enable. Default value: 1. (0: Z-axis output disabled; 1: Z-axis output enabled)
Yen_XL	Accelerometer's Y-axis output enable. Default value: 1. (0: Y-axis output disabled; 1: Y-axis output enabled)
Xen_XL	Accelerometer's X-axis output enable. Default value: 1. (0: X-axis output disabled; 1: X-axis output enabled)

6.21 CTRL10_C (19h)

Control Register 10 (r/w).

Table 66. CTRL10_C register

0(1)	0(1)	Zen_G	Yen_G	Xen_G	DCRM_XL	LIR_XL	4D_XL

1. This bit must be set to '0' for the correct operation of the device.

Table 67. CTRL10_C register description

Zen_G	Gyroscope's yaw axis (Z) output enable. Default value: 1. (0: Z-axis output disabled; 1: Z-axis output enabled)
Yen_G	Gyroscope's roll axis (Y) output enable. Default value: 1. (0: Y-axis output disabled; 1: Y-axis output enabled)
Xen_G	Gyroscope's pitch axis (X) output enable. Default value: 1. (0: X-axis output disabled; 1: X-axis output enabled)
DCRM_XL	Interrupt duration counter reset mode selection. Default value: 0. (0: counter is reset; 1: duration counter is decremented by 1LSB)
LIR_XL	Latched interrupt. Default value: 0. (0: interrupt request not latched; 1: interrupt request latched)
4D_XL	4D option enabled on Interrupt. Default value: 0. (0: interrupt generator uses 6D for position recognition; 1: interrupt generator uses 4D for position recognition)

6.22 FIFO_CTRL (1Ah)

FIFO Control Register (r/w).

Table 68. FIFO_CTRL register

FMODE2	FMODE1	FMODE0	FTH4	FTH3	FTH2	FTH1	FTH0

Table 69. FIFO_CTRL register description

FMODE [2:0]	FIFO mode selection bits. Default value: 000. For further details refer to *Table 70*.
FTH [4:0]	FIFO threshold level setting. Default value: 0 0000.

Table 70. FIFO mode selection

FMODE2	FMODE1	FMODE0	Mode
0	0	0	Bypass mode. FIFO turned off
0	0	1	FIFO mode. Stop collecting data when FIFO is full.
0	1	0	Stream mode. If the FIFO is full, the new sample overwrites the older sample.
0	1	1	Stream mode until trigger is deasserted, then FIFO mode.
1	0	0	Bypass mode until trigger is deasserted, then Stream mode.
1	1	0	Dynamic Stream mode.

6.23 INT_SRC_XL (1Dh)

Linear acceleration sensor interrupt source register. Read-only register.

Table 71. INT_SRC_XL register

0	IA_XL	ZH_XL	ZL_XL	YH_XL	YL_XL	XH_XL	XL_XL

Table 72. INT_SRC_XL register description

IA_XL	Interrupt active. (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH_XL	Accelerometer's Z high event. (0: no interrupt, 1: Z high event has occurred)
ZL_XL	Accelerometer's Z low event. (0: no interrupt; 1: Z low event has occurred)
YH_XL	Accelerometer's Y high event. (0: no interrupt, 1: Y high event has occurred)
YL_XL	Accelerometer's Y low event. (0: no interrupt, 1: Y low event has occurred)
XH_XL	Accelerometer's X high event. (0: no interrupt, 1: X high event has occurred)
XL_XL	Accelerometer's X low event. (0: no interrupt, 1: X low event has occurred)

6.24 FIFO_SRC (1Eh)

FIFO status control register (r).

Table 73. FIFO_SRC register

FTH	OVRN	FSS5	FSS4	FSS3	FSS2	FSS1	FSS0

Table 74. FIFO_SRC register description

FTH	FIFO threshold status. (0: FIFO filling is lower than threshold level; 1: FIFO filling is equal to or higher than threshold level
OVRN	FIFO overrun status. (0: FIFO is not completely filled; 1: FIFO is completely filled and at least one sample has been overwritten) For further details refer to *Table 75*.
FSS [5:0]	Number of unread samples stored in FIFO. (000000: FIFO empty; 100000: FIFO full, 32 unread samples) For further details refer to *Table 75*.

Table 75. FIFO_SRC example: OVR/FSS details

FTH	OVRN	FSS5	FSS4	FSS3	FSS2	FSS1	FSS0	Description
0	0	0	0	0	0	0	0	FIFO empty
--(1)	0	0	0	0	0	0	1	1 unread sample
...								
--(1)	0	1	0	0	0	0	0	32 unread sample
1	1	1	0	0	0	0	0	At least one sample has been overwritten

1. When the number of unread samples in FIFO is greater than the threshold level set in register *FIFO_CTRL (1Ah)*, FTH value is '1'.

6.25 STATUS_REG (1Fh)

Status register (r).

Table 76. STATUS_REG register

0	IG_XL	0	INACT	BOOT_ STATUS	TDA	GDA	XLDA

Table 77. STATUS_REG register description

IG_XL	Accelerometer interrupt output signal. (0: no interrupt has been generated; 1: one or more interrupt events have been generated)
INACT	Inactivity interrupt output signal. (0: no interrupt has been generated; 1: one or more interrupt events have been generated)
BOOT_ STATUS	Boot running flag signal. (0: no boot running; 1: boot running)
TDA	Temperature sensor new data available. (0: a new data is not yet available; 1: a new data is available)
GDA	Gyroscope new data available. (0: a new set of data is not yet available; 1: a new set of data is available)
XLDA	Accelerometer new data available. (0: a new set of data is not yet available; 1: a new set of data is available)

6.26 OUT_TEMP_L (20h), OUT_TEMP_H (21h)

Temperature data output register (r). L and H registers together express a 16-bit word in two's complement right aligned.

Table 78. OUT_TEMP_L register

Temp7	Temp6	Temp5	Temp4	Temp3	Temp2	Temp1	Temp0

Table 79. OUT_TEMP_H register

Temp11	Temp11	Temp11	Temp11	Temp11	Temp10	Temp9	Temp8

Table 80. OUT_TEMP register description

Temp [11:0]	Temperature sensor output data. The value is expressed as two's complement sign extended on the MSB.

6.27 OUTX_G (22h - 23h)

Angular rate sensor pitch axis (X) angular rate output register (r). The value is expressed as a 16-bit word in two's complement.

6.28 OUTY_G (24h - 25h)

Angular rate sensor roll axis (Y) angular rate output register (r). The value is expressed as a 16-bit word in two's complement.

6.29 OUTZ_G (26h - 27h)

Angular rate sensor yaw axis (Z) angular rate output register (r). The value is expressed as a 16-bit word in two's complement.

6.30 OUTX_XL (28h - 29h)

Linear acceleration sensor X-axis output register (r). The value is expressed as a 16-bit word in two's complement.

6.31 OUTY_XL (2Ah - 2Bh)

Linear acceleration sensor Y-axis output register (r). The value is expressed as a 16-bit word in two's complement.

6.32 OUTZ_XL (2Ch - 2Dh)

Linear acceleration sensor Z-axis output register (r). The value is expressed as a 16-bit word in two's complement.

6.33 LPF_BYP_REG (33h)

LPF2 selection register (r/w).

Table 81. LPF_BYP_REG register

LPF_BYP	0	0	0	0	0	0	0

Table 82. LPF_BYP_REG register description

LPF_BYP	Digital low-pass filter selection. Default value: 0 (0: digital low-pass filter enabled; 1: digital low-pass filter bypassed)

7 Soldering information

The LGA package is compliant with the ECOPACK®, RoHS and "Green" standard.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Leave "Pin 1 Indicator" unconnected during soldering.

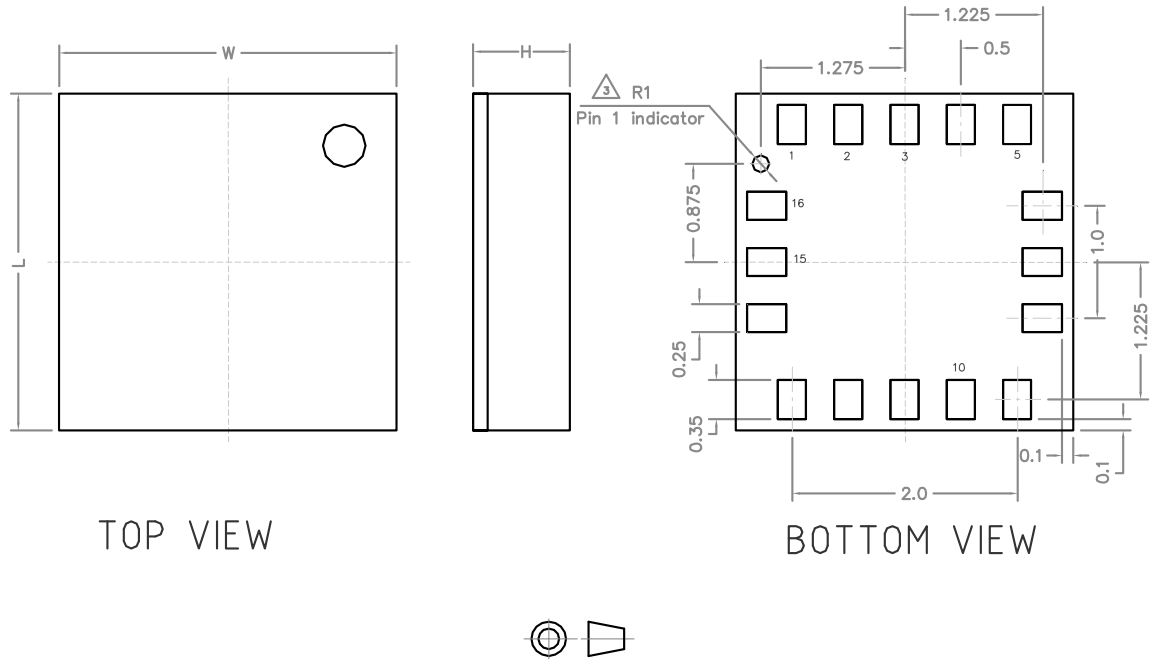
Land pattern and soldering recommendations are available at www.st.com/mems.

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

8.1 LGA package information

Figure 23. LGA-16 3x3x1.1 package outline and dimensions



Dimensions are in millimeter unless otherwise specified
General Tolerance is +/-0.1mm unless otherwise specified

OUTER DIMENSIONS

ITEM	DIMENSION [mm]	TOLERANCE [mm]
Length [L]	3.00	±0.1
Width [W]	3.00	±0.1
Height [H]	1.1	Typ

8574403_B

9 Revision history

Table 83. Document revision history

Date	Revision	Changes
25-Feb-2015	1	Initial release
16-Mar-2015	2	Added *Section 6.33: LPF_BYP_REG (33h)* and updated *Table 17*
23-Oct-2015	3	Updated pin 6 and 7 in *Figure 1: Pin connections* and *Table 2* Added sinc filter gyro to *Figure 7: Block diagram* Updated *CTRL3_C (12h)*