SENSORAY CO., INC.

Multifunctional I/O Board

Model 526 (Rev.A)

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Limited warranty

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The warranty provided herein does not cover equipment subjected to abuse, misuse, accident, alteration, neglect, or unauthorized repair or installation. Sensoray shall have the right of final determination as to the existence and cause of defect.

As for items repaired or replaced under warranty, the warranty shall continue in effect for the remainder of the original warranty period, or for ninety days following date of shipment by Sensoray of the repaired or replaced part, whichever period is longer.

A Return Material Authorization (RMA) number must be obtained from the factory and clearly marked on the outside of the package before any equipment will be accepted for warranty work. Sensoray will pay the shipping costs of returning to the owner parts that are covered by warranty. A restocking charge of 25% of the product purchase price, or $105, whichever is less, will be charged for returning a product to stock.

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Special handling instructions

The circuit board contains CMOS circuitry that is sensitive to Electrostatic Discharge (ESD). Special care should be taken in handling, transporting, and installing circuit board to prevent ESD damage to the board. In particular:

- Do not remove the circuit board from its protective anti-static bag until you are ready to install the board into the enclosure.
- Handle the circuit board only at grounded, ESD protected stations.
- Remove power from the equipment before installing or removing the circuit board.

Introduction

Model 526 is a PC/104 multifunctional I/O board with the following features:

- Four 24-bit programmable counters. Inputs could be driven from incremental encoders (in 1x, 2x, or 4x modes) or any digital signal. Inputs accept differential (RS-422) or standard TTL/CMOS single-ended signals. The counters can also count internal clock (27 or 13.5 MHz).
- Eight digital I/O channels configurable as inputs or outputs (in groups of 4) and capable of generating interrupts.
- 4-channel 16-bit D/A converter (±10 V).
- 8-channel (multiplexed) differential 16-bit A/D converter (±10 V).
- Programmable interrupt timer.
- Watchdog timer with configurable timeout and output.
- EEPROM for calibration data storage.
- Flexible address and interrupt line configuration.
- Requires one power supply (+5V).

Model 526 is controlled through a set of 27 registers mapped into I/O space. The base address of the board is selected with jumpers from a range of 0x0000 to 0xFFC0. The board is shipped with the base address set to 0x2C0. All register accesses are 16 bit; 1 byte and odd address accesses are not supported.

Model 526 can generate interrupts on various programmable conditions. The interrupt line used by the board is selected with jumpers from the following IRQ values: 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 and 15. The board is shipped with the interrupt set to IRQ3.

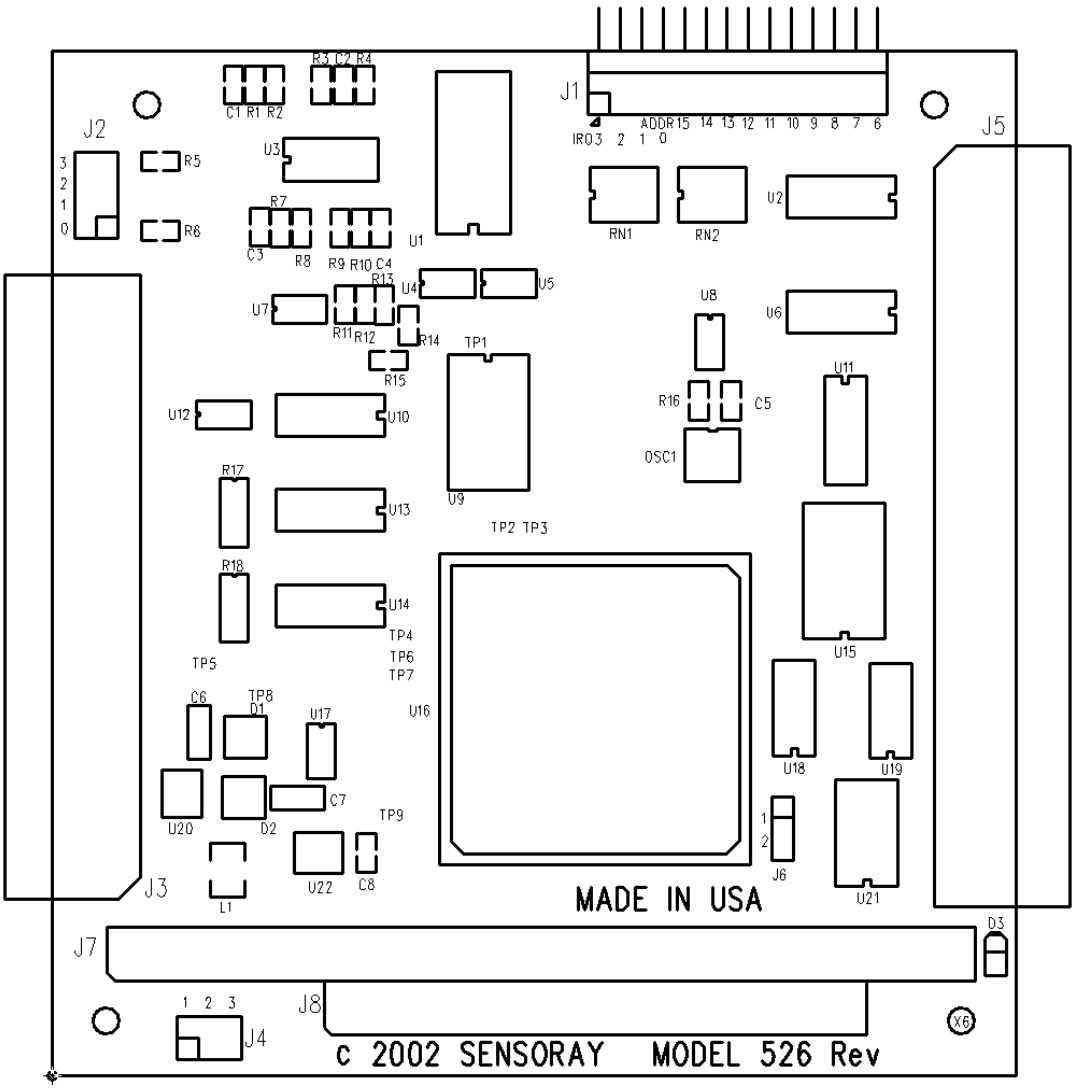

Fig.1. Model 526 board outline.

Programmable Counters

Model 526 contains 4 identical 24-bit up/down counters with enable and preload. The block diagram of one of the counters is shown on Fig.2.

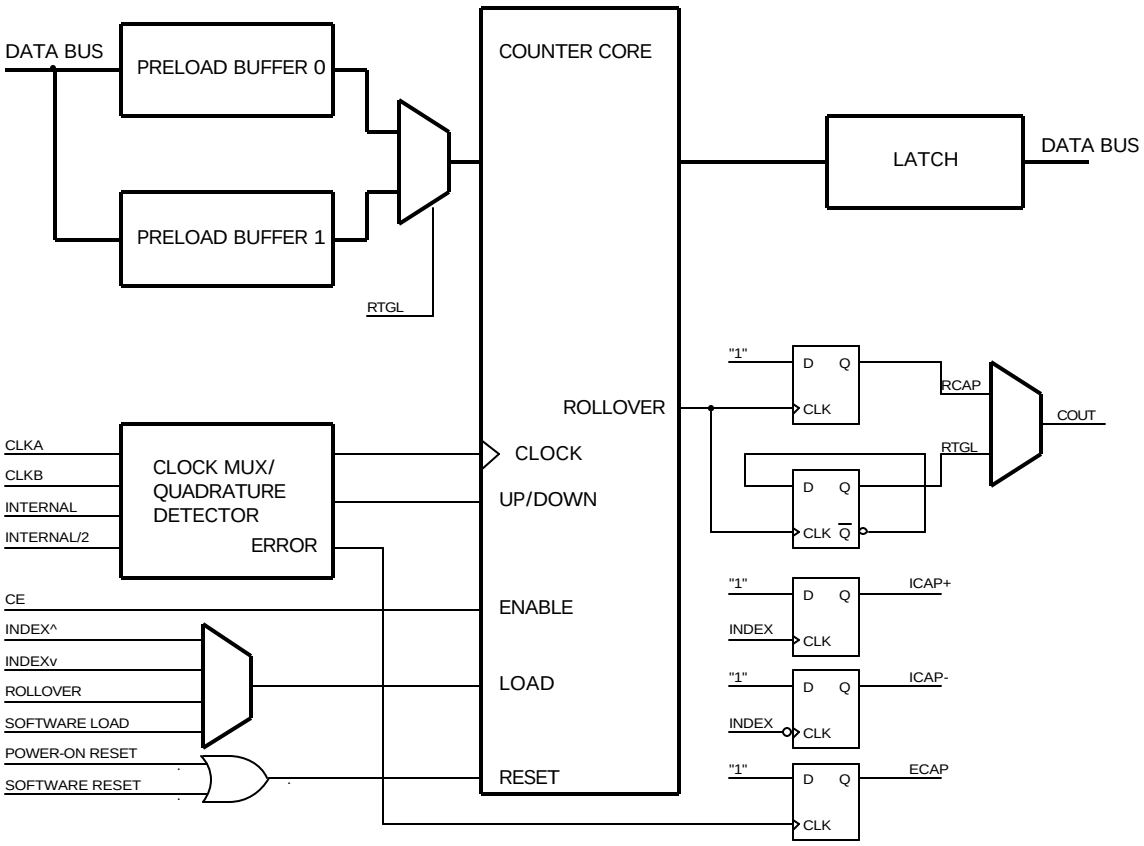

Fig.2. Counter simplified block diagram.

See the description of Counter Mode register and Counter Control/Status register in the **Registers** section for the implementation specifics.

Input Signals

The counter accepts the following input signals (connector J5):

- CLKA – phase A of the encoder, or any clock signal in normal mode;
- CLKB – phase B of the encoder;
- INDEX – index signal of the encoder, or any digital signal;
- CE – external count enable.

Signals CLKA, CLKB and INDEX could be either differential (RS-422), or single-ended. In case of a single-ended signal the "+" input has to be used.

The clock source can be selected through the software. In quadrature mode the possible clock sources are:

- quadrature x1 (CLKA↑ counting up, CLKA↓ counting down);

- quadrature x2 (both edges of CLKA);
- quadrature x4 (both edges of both CLKA and CLKB);

In normal mode the clock sources are:
- CLKA↑;
- CLKA↓;
- Internal clock (27 MHz);
- Internal clock divided by 2 (13.5 MHz).

Count direction (up or down) is set through the software (normal mode) or determined from CLKA-CLKB phase relationship (quadrature mode).

Count is enabled either through the software, or with the external signal. Possible sources of Count Enable signal are:
- CEN;
- INDEX;
- INDEX↑ to INDEX↓ (count does not start until the rising edge of INDEX signal);
- NOT RCAP (see the description of RCAP signal below).

The polarity of Count Enable signal can be inverted through the software.

Captured Events

The counter detects or generates the following "short" events:
- RO – rollover, counter overflow (when counting up) or underflow (when counting down);
- INDEX↑ - rising edge of INDEX signal;
- INDEX↓ - falling edge of INDEX signal;
- ERROR – illegal quadrature state transition.

"Short" events can generate interrupts, if enabled.

To facilitate reliable detection by the software, the "short" events are captured (see Fig.2), thus generating corresponding captured events:
- RCAP – captured RO signal;
- ICAP+ - captured rising edge of INDEX signal;
- ICAP- - captured falling edge of INDEX signal;
- ECAP – captured ERROR signal.

Captured events status can be read and reset through the Control/Status Register.

Additionally, RO generates RTGL – a signal which toggles each time rollover is generated.

Output Signals

The following signals can be routed to the counter output signal (COUT):
- RCAP;
- RTGL.

The polarity of COUT signal can be inverted through the software.

Counter Preload

Each counter has 2 preload registers accessible individually through the software, PR0 and PR1. The counter is loaded from a preload register under software control (from PR0), or automatically. The preload register from which the counter is loaded in automatic mode is

determined by the state of the RTGL signal: PR0 when RTGL is low, PR1 when RTGL is high. The autoload occurs under a programmable combination of the following conditions:

- INDEX↑ - rising edge of INDEX signal;
- INDEX↓ - falling edge of INDEX signal;
- RO – rollover.

See application examples below for the explanation of preload registers usage.

The preload registers are 24 bits long, so they can not be written to with one operation. In order to prevent the situation when the counter is loaded with incomplete data, an intermediate buffer holds the high word of a preload register until the data is written to the low word, so that both high and low words are written to the preload register simultaneously. Thus the high word has to be always written first.

Output Register

Counter output data (24-bit) requires 2 read accesses to be read out. To ensure that all bits of the reading correspond to the same instant each counter has an output register. The data can be latched into the output register either by a read access to the low word of Counter Data register, or by a hardware event, depending on the state of "Output register latch control" bit of the Counter Mode register. The hardware event that can latch the counter data is a logical OR of any of the following: INDEX rising edge, INDEX falling edge, interrupt timer expiration.

Latching the data into the output register does not interrupt the count. Latching on read access occurs on the access to the low word, so in case "Latch on read" mode is selected the low word has to be always read first.

Examples of Counter Applications

All the following examples assume the use of counter 0. The pseudocode function RegisterWrite(address, data) has a meaning of writing a 2-byte word *data* to I/O address (*base+address*), where *base* is the base I/O address of the board.

One-shot (software trigger)

In this mode the counter clock source is set to internal, so the length of the generated pulse is expressed in units of 1/27 MHz ≈ 37 ns. Assuming the desired positive going pulse length is 3 ms the counter has to be loaded with the value of 3 ms x 27 MHz = 81,000 = 0x13C68. The Count Enable is set to NOT RCAP, the counter output (COUT) to RCAP with COUT polarity inverted.

Step 1. Load the preload register PR0 with 0x13C68. First, set the Counter Mode register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	1	1	0	1	0	1	1	0	0	0	1	0
X	PR0	X	Soft count direction control	Count direction: down	Clock source: internal		Count enable: hardware		NOT RCAP		Auto load: disable			Polarity: inverted	Out: RCAP

```
// select PR0 as a target for Preload register access
// set operating mode, don't enable count yet
RegisterWrite (0x16, 0x1D62); //load Counter Mode register
```

```
RegisterWrite (0x14, 0x0001); //load Preload Register high word
RegisterWrite (0x12, 0x3C68); //load Preload Register low word
```

Step 2. Reset the counter (to clear RTGL), load the counter from Preload Register 0.

```
RegisterWrite (0x18, 0x8000); //reset the counter
RegisterWrite (0x18, 0x4000); //load the counter from PR0
```

Step 3. Reset RCAP (fires one-shot).

```
RegisterWrite (0x18, 0x8);
```

One-shot (hardware trigger)

The following example shows how to fire the one-shot on the positive edge of external trigger. The trigger signal is connected to the INDEX input of the counter.

Step 1. Load both preload registers PR0 and PR1 with 0x13C68. First, set the Counter Mode register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	1	1	0	1	0	1	1	1	0	0	1	0
X	PR0	X	Soft count direction control	Count direction: down	Clock source: internal		Count enable: hardware		NOT RCAP		Auto load and reset RCAP: INDEX↑			Polarity: inverted	Out: RCAP

```
// select PR0 as a target for Preload register access
// do not enable autoload (bit 4) yet
RegisterWrite (0x16, 0x1D62); //load Counter Mode register
RegisterWrite (0x14, 0x0001); //load Preload Register 0 high word
RegisterWrite (0x12, 0x3C68); //load Preload Register 0 low word
// select PR1 as a target for Preload register access
RegisterWrite (0x16, 0x5D62); //load Counter Mode register
RegisterWrite (0x14, 0x0001); //load Preload Register 1 high word
RegisterWrite (0x12, 0x3C68); //load Preload Register 1 low word
```

Step 2.

```
// enable autoload
RegisterWrite (0x16, 0x3D72); //load Counter Mode register
```

Pulse Width Modulation

Let's assume the following requirements:
Period = 10 ms; "high" state = 2 ms; "low" state = 8 ms. Then the "high" length in periods of the 27 MHz clock is 2 ms x 27 MHz = 54000 = 0xD2F0, the "low" length is 8 ms x 27 MHz = 216000 = 0x34BC0.

Step 1. Load Preload Register 0.

```
// select PR0 as a target for Preload register access, load PR0
RegisterWrite (0x16, 0x1C85); //load Counter Mode register
RegisterWrite (0x14, 0x0003); //load Preload Register 0 high word
RegisterWrite (0x12, 0x4BC0); //load Preload Register 0 low word
```

Step 2. Load Preload Register 1.

```
// select PR1 as a target for Preload register access, load PR1
RegisterWrite (0x16, 0x5C85); //load Counter Mode register
RegisterWrite (0x14, 0x0000); //load Preload Register 0 high word
RegisterWrite (0x12, 0xD2F0); //load Preload Register 0 low word
```

To change the duty cycle steps 1-2 have to be repeated with the new preload register values.

Interrupt Timer

The interrupt timer provides a way of generating interrupts at precise time intervals in the range between approximately 100 µs and 25.5 ms. The timer is an 8-bit down counter with a preload counting a 99.852 µs clock. Two operation modes are available: manual restart and autorestart. In the manual restart mode the count starts on a software command and stops when the zero count is reached. In autorestart mode the counter automatically reloads and restarts after the zero count is reached.

Bit [0] of the Interrupt Status Register is set when the timer expires, and an interrupt is generated if bit [0] of the Interrupt Enable Register is set to 1.

Interrupt timer expiration event can latch the output data of the counter(s), if this option is enabled in Counter Control/Status Register(s).

Watchdog Timer

The watchdog timer has a timeout value programmable in 8 steps between 0.125 s and 16 s. If enabled, the watchdog timer times out after a selected time interval if it is not “tagged”. Reading the watchdog timer register “tags” it (restarts the count).

The watchdog timer generates a signal that controls a set of 2 solid-state relays (one normally open, one normally closed) (Fig.3). Inserting a shunt in position 1-2 of jumper J6 selects a normally open relay, inserting it in position 2-3 selects a normally closed relay.

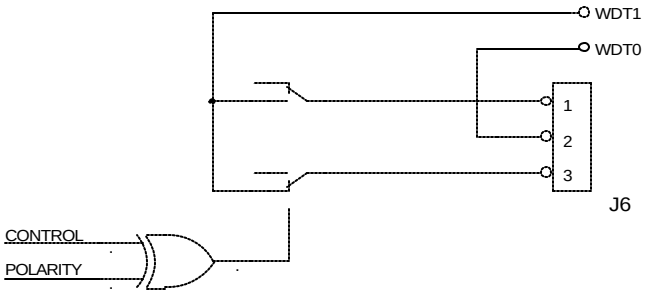

Fig.3. Watchdog timer output circuit.

For additional flexibility the operating mode of the watchdog timer is controlled by 2 bits of the Watchdog Timer Control register and 2 jumpers.

Watchdog enable/disable

Watchdog enable/disable is controlled by bit [3] of the Watchdog Timer Control register and jumper 1 of J4.

Shunt in position 1 of J4	Bit [3] of Control Register	Watchdog timer
Not installed	0	Disabled
Not installed	1	Enabled
Installed	0	Enabled
Installed	1	Disabled

Bit [3] is always 0 after power up, so if the watchdog timer has to be enabled by default, the shunt has to be installed.

Solid-sate relay control

The polarity of the watchdog timer output signal (CONTROL on Fig.3) is controlled by bit [4] of the Watchdog Timer Control register and jumper 2 of J4. When CONTROL is not active, each solid-state relay is in its default (normal) state. When CONTROL becomes active, the solid-state relays change their states.

Shunt in position 2 of J4	Bit [4] of Control Register	Solid-state relay control	
		Timed out	Not timed out
Not installed	0	Active	Not active
Not installed	1	Not active	Active
Installed	0	Not active	Active
Installed	1	Active	Not active

D/A Converter

Model 526 implements a 4-channel 16-bit D/A converter. Each channel has an individual preload buffer. Preload buffers are accessed through a single write register (DAC/ADC Data register) and selected with 2 bits of the DAC Control register. Upload to the DAC is performed for all 4 channels from their corresponding preload buffers with a single software command and takes approximately 8 μs to complete. A bit in the Interrupt Status register is set when the upload is complete, and an interrupt is generated, if enabled in the Interrupt Enable register. See the description of DAC Control register in the **Registers** section for the implementation specifics.

The DAC range is slightly wider than ±10 V which allows for software calibration. The code value of 0 corresponds to the most negative output voltage, the code value of 0xFFFF corresponds to the most positive output voltage.

Calibration

The D/A converter is calibrated at the factory. For each of the 4 channels 2 coefficients are stored in the on-board EEPROM: a and b, such that the digital code that has to be loaded to the DAC in order to obtain output voltage V is equal to $C = a \cdot V + b$, where V is in volts. The constants are stored in the **`double`** floating point format (8 bytes per value). See the ***Calibration EEPROM*** section for the details.

A/D Converter

Model 526 implements an 8-channel multiplexed differential 16-bit A/D converter. The input signal range is slightly wider than ±10 V which allows for software calibration. Multiple channels can be digitized with one software command. Bits [14:5] of the ADC Control register allow selection of any combination of 8 input channels and 2 reference channels (0 V and +10V). Each of 10 digitized channels has its own buffer register. The buffer registers are accessed through a single read register (DAC/ADC Data register) and selected with 4 bits of the ADC Control register. A bit in the Interrupt Status register is set when the conversion is complete, and an interrupt is generated, if enabled in the Interrupt Enable register. See the description of ADC Control register in the **Registers** section for the implementation specifics.

As long as the ADC inputs are multiplexed, a multiplexor settling delay of approximately 15 μs is provided automatically before each measurement. A bit in the ADC Control register allows turning this delay off, which increases sampling rate in case of the repetitive measurements from a single channel.

The output code of the ADC is binary two's complement; the most positive input voltage produces a code of 0x3FFF, the most negative input voltage produces a code of 0x8000.

Calibration

The A/D converter is calibrated at the factory. One calibration constant is stored in the on-board EEPROM: the actual value of the on-board 10V reference. In order to obtain accurate reading of the input signal a normalization procedure has to be performed first: values of the on-board +10V reference and 0V reference have to be measured. (Those values and the input values could be measured using a single command. See the description of the A/D Control register for the details). The actual value of the measured voltage is then obtained as

$$V_{meas} = V_{ref} \cdot \left(\frac{C_{meas} - C_0}{C_{ref} - C_0} \right),$$

where

V_{ref} - the actual value of the on-board 10V reference (from the EEPROM);

C_{meas} - ADC reading corresponding to the measured voltage;

C_{ref} - ADC reading corresponding to the on-board +10V reference;

C_0 - ADC reading corresponding to the on-board 0V reference.

The calibration constant is stored in the **`double`** floating point format (8 bytes per value). See the ***Calibration EEPROM*** section for the details.

Digital I/O

Digital I/O on model 526 consists of 8 signals, which can be configured as inputs or outputs in groups of 4: DIO group 1 (DIO0-3) and DIO group 2 (DIO4-7). Interrupts can be generated on rising or falling edges of DIO signals. Interrupt condition (rising or falling edge) can be selected individually for every signal in group 1, and for group 2 as a whole. See Digital I/O Control register description in the **Registers** section for the details.

Interrupts

Interrupts are controlled with 2 registers: Interrupt Enable register (IER) and Interrupt Status register (ISR). ISR stores the status of various events, IER enables or disables the ability of those events to generate an interrupt (Fig.4).

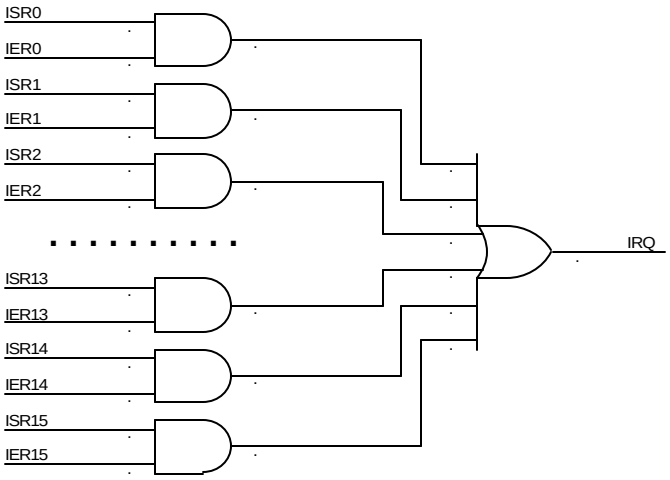

Fig.4. Simplified diagram of the interrupt controller.

When a specific interrupt condition is met, a corresponding bit is set in the ISR. If an interrupt was enabled for this source by setting a corresponding bit of the IER to 1, the signal on the board's interrupt pin (selected with jumpers) goes high, generating an ISA interrupt. An interrupt handler (software) must immediately disable the interrupts by writing a value of 0x0000 to the IER, which results in the signal on the board's interrupt pin going low. Next an interrupt handler detects the source of the interrupt by analyzing the ISR, and resets the corresponding bits. (Note that the ISR bits corresponding to the counters' interrupt status are reset by resetting the corresponding bits in the Counter Control/Status registers). When the interrupt processing is over, the interrupt handler must restore the value of the IER. If a bit of the ISR has been set to 1 while the interrupt handler was processing previous interrupt(s), the IRQ signal will go high again immediately after the IER is restored, so no interrupts are lost.

Calibration EEPROM

An on-board EEPROM is provided for calibration data storage. Data from the EEPROM is read by using a set of 2 registers: EEPROM Command/Status register and EEPROM data register. The EEPROM is organized as 64 2-byte words, with addresses from 0x00 to 0x3F. The address map of the EEPROM is as following:

Address	Contents
0x00	DAC channel 0 parameter ***a*** (bits [15:0])
0x01	DAC channel 0 parameter ***a*** (bits [31:16])
0x02	DAC channel 0 parameter ***a*** (bits [47:32])
0x03	DAC channel 0 parameter ***a*** (bits [63:48])
0x04	DAC channel 0 parameter ***b*** (bits [15:0])
0x05	DAC channel 0 parameter ***b*** (bits [31:16])
0x06	DAC channel 0 parameter ***b*** (bits [47:32])
0x07	DAC channel 0 parameter ***b*** (bits [63:48])
0x08	DAC channel 1 parameter ***a*** (bits [15:0])
0x09	DAC channel 1 parameter ***a*** (bits [31:16])
0x0A	DAC channel 1 parameter ***a*** (bits [47:32])
0x0B	DAC channel 1 parameter ***a*** (bits [63:48])
0x0C	DAC channel 1 parameter ***b*** (bits [15:0])
0x0D	DAC channel 1 parameter ***b*** (bits [31:16])
0x0E	DAC channel 1 parameter ***b*** (bits [47:32])
0x0F	DAC channel 1 parameter ***b*** (bits [63:48])
0x10	DAC channel 2 parameter ***a*** (bits [15:0])
0x11	DAC channel 2 parameter ***a*** (bits [31:16])
0x12	DAC channel 2 parameter ***a*** (bits [47:32])
0x13	DAC channel 2 parameter ***a*** (bits [63:48])
0x14	DAC channel 2 parameter ***b*** (bits [15:0])
0x15	DAC channel 2 parameter ***b*** (bits [31:16])
0x16	DAC channel 2 parameter ***b*** (bits [47:32])
0x17	DAC channel 2 parameter ***b*** (bits [63:48])
0x18	DAC channel 3 parameter ***a*** (bits [15:0])
0x19	DAC channel 3 parameter ***a*** (bits [31:16])
0x1A	DAC channel 3 parameter ***a*** (bits [47:32])
0x1B	DAC channel 3 parameter ***a*** (bits [63:48])
0x1C	DAC channel 3 parameter ***b*** (bits [15:0])
0x1D	DAC channel 3 parameter ***b*** (bits [31:16])
0x1E	DAC channel 3 parameter ***b*** (bits [47:32])
0x1F	DAC channel 3 parameter ***b*** (bits [63:48])
0x20	ADC reference value (bits [15:0])
0x21	ADC reference value (bits [31:16])
0x22	ADC reference value (bits [47:32])
0x23	ADC reference value (bits [63:48])

See **A/D** and **D/A Converter** sections for the details of the calibration procedures.

Configuration Jumpers

A set of configuration jumpers (J1) allows selection of board's base address and interrupt line (See Fig.1).

Jumpers marked ADDR15-6 select the higher 10 bits of the board's base address in I/O space. Inserted jumper sets the corresponding bit to 0. The board ships with base address set to 0x2C0.

Jumpers marked IRQ3-0 select the interrupt line used by the board. Inserted jumper means a corresponding bit in the 4-digit binary representation of the interrupt number is set to 0. For example, inserting jumpers 2 and 0 sets the interrupt line used by the board to IRQ10. The board can use the following interrupt lines: 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 and 15. All other combinations are not allowed. The board ships with the interrupt set to IRQ3.

Jumpers J4 and J6 are used to configure the watchdog timer. See the corresponding section for the details.

Connectors

Analog connector (J3)

Pin	Signal	Pin	Signal
1	Ground	2	Ground
3	Analog input 0 (-)	4	Analog input 0 (+)
5	Analog input 1 (-)	6	Analog input 1 (+)
7	Analog input 2 (-)	8	Analog input 2 (+)
9	Analog input 3 (-)	10	Analog input 3 (+)
11	Analog input 4 (-)	12	Analog input 4 (+)
13	Analog input 5 (-)	14	Analog input 5 (+)
15	Analog input 6 (-)	16	Analog input 6 (+)
17	Analog input 7 (-)	18	Analog input 7 (+)
19	Ground	20	Ground
21	Ground	22	Ground
23	Analog output 0	24	Feedback 0
25	Return 0 (Ground)	26	Ground
27	Analog output 1	28	Feedback 1
29	Return 1 (Ground)	30	Ground
31	Analog output 2	32	Feedback 2
33	Return 2 (Ground)	34	Ground
35	Analog output 3	36	Feedback 3
37	Return 3 (Ground)	38	Ground
39	Ground	40	Ground

Notes:

1. Pins Return 0-3 are connected to ground on the board.
2. If the feedback for an analog output is provided through a Feedback pin of J3, the corresponding shunt on jumper J2 has to be removed. Otherwise the shunt has to be installed, and the feedback is taken directly from the output of the DAC.

Digital connector (J5)

Pin	Signal	Pin	Signal
1	Clock A 0 -	2	Clock A 0 +
3	Clock B 0 -	4	Clock B 0 +
5	Index 0 -	6	Index 0 +
7	Count Enable 0	8	Counter Output 0
9	Encoder 0 power (+5V)	10	Ground
11	Clock A 1 -	12	Clock A 1 +
13	Clock B 1 -	14	Clock B 1 +
15	Index 1 -	16	Index 1 +
17	Count Enable 1	18	Counter Output 1
19	Encoder 1 power (+5V)	20	Ground
21	Clock A 2 -	22	Clock A 2 +
23	Clock B 2 -	24	Clock B 2 +
25	Index 2 -	26	Index 2 +
27	Count Enable 2	28	Counter Output 2
29	Encoder 2 power (+5V)	30	Ground
31	Clock A 3 -	32	Clock A 3 +
33	Clock B 3 -	34	Clock B 3 +
35	Index 3 -	36	Index 3 +
37	Count Enable 3	38	Counter Output 3
39	Encoder 3 power (+5V)	40	Ground
41	DIO0	42	DIO1
43	DIO2	44	DIO3
45	DIO4	46	DIO5
47	DIO6	48	DIO7
49	WDT relay 0	50	WDT relay 1

Notes:

1. Clock A, Clock B and Index are differential inputs for the encoders. The “+” input has to be used for single-ended signals.
2. Encoder power is provided from a +5V source protected by a single resettable fuse rated at 1.1A.

Registers

Register Map

Register addresses are relative to the base address selected with address jumpers (ADDR 15 – 6). All register accesses are 2-byte. Single byte and odd address accesses are not supported.

Address		Write	Read
0x00	TCR	Timer control register	
0x02	WDC	Watchdog timer control register	
0x04	DAC	DAC control	
0x06	ADC	ADC control	
0x08	ADD	DAC data	ADC data
0x0A	DIO	Digital I/O control	Digital I/O data
0x0C	IER	Interrupt enable register	
0x0E	ISR	Interrupt status register	Interrupt status register
0x10	MSC	Miscellaneous register	Miscellaneous register
0x12	C0L	Counter 0 preload register low word	Counter 0 data low word
0x14	C0H	Counter 0 preload register high word	Counter 0 data high word
0x16	C0M	Counter 0 mode register	
0x18	C0C	Counter 0 control register	Counter 1 status register
0x1A	C1L	Counter 1 preload register low word	Counter 1 data low word
0x1C	C1H	Counter 1 preload register high word	Counter 1 data high word
0x1E	C1M	Counter 1 mode register	
0x20	C1C	Counter 1 control register	Counter 1 status register
0x22	C2L	Counter 2 preload register low word	Counter 1 data low word
0x24	C2H	Counter 2 preload register high word	Counter 1 data high word
0x26	C2M	Counter 2 mode register	
0x28	C2C	Counter 2 control register	Counter 2 status register
0x2A	C3L	Counter 3 preload register low word	Counter 2 data low word
0x2C	C3H	Counter 3 preload register high word	Counter 2 data high word
0x2E	C3M	Counter 3 mode register	
0x30	C3C	Counter 3 control register	Counter 3 status register
0x32	EED	EEPROM data	EEPROM data
0x34	EEC	EEPROM interface command	Signature

The following signal types and default values are used to specify registers implementation:

RW read/write;
WO write only (data read may not be the same as data written);
RR read/reset (writing a 1 resets the corresponding bit to 0, writing a 0 has no effect);
RO read only;
UU unused.

0 the value after a hardware reset is 0;
1 the value after a hardware reset is 1;
X “don’t care” for write, undefined for read.

Timer Control Register
0x00

Bits	Type	Default	Description
[15:8]	WO	0x00	Timer preload data in 100 us ticks.
[7:2]	UU	XXXXXX	Reserved
[1]	WO	0	Timer mode: 0 – manual restart; 1 – auto restart.
[0]	WO	0	Manual restart. Writing a 1 restarts the timer if [1] is 0. Bit [0] of the Interrupt Status register is set to 1 when timer expires.

Watchdog Timer Control Register
0x02

Bits	Type	Default	Description
[15:5]	UU	X	Reserved.
[4]	WO	0	Solid-state relay control signal polarity: 0 – normal (active when timed out), 1 – inverted (active when not timed out). (See Note 2).
[3]	WO	0	Watchdog timer software enable: writing a 1 enables, writing a 0 disables the watchdog timer (see Note 3).
[2:0]	WO	000	Timeout interval: 000 – 16 sec; 001 – 8 sec; 010 – 4 sec; 011 – 2 sec; 100 – 1 sec; 101 – 0.5 sec; 110 – 0.25 sec; 111 – 0.125 sec.

Notes:
1. Reading the Watchdog Timer Control register “tags” the watchdog (restarts the count). The data returned by read access is undefined.
2. The meaning of bit [4] corresponds to the case when a shunt in position 2 of jumper J4 is NOT installed. If the shunt is installed, the meaning of bit [4] is reversed: 0 corresponds to normal, and 1 – to inverted polarity of the solid-state relay control signal.
3. The meaning of bit [3] corresponds to the case when a shunt in position 1 of jumper J4 is NOT installed. If the shunt is installed, the meaning of bit [3] is reversed: 0 enables, and 1 disables the watchdog timer. Thus installing the shunt enables the watchdog timer by default after the power up.

DAC Control Register

0x04

Bits	Type	Default	Description
[15:4]	UU	X	Reserved.
[3]	WO	0	DAC reset. Writing a 1 to this bit resets all DAC channels. Writing a 0 has no effect.
[2:1]	WO	00	DAC data buffer select. Write accesses to DAC Data Register are routed to the corresponding data buffer: 00 - channel 0; 01 - channel 1; 10 - channel 2; 11 - channel 3;
[0]	WO	0	DAC start. Writing a 1 to this bit starts upload for all DAC channels. Bit [1] of the Interrupt Status register is set to 1 when upload is complete.

ADC Control Register
0x06

Bits	Type	Default	Description
[15]	WO	0	Input multiplexor settling delay: 0 – no delay; 1 – 12 μs delay.
[14:5]	WO	0x000	ADC conversion control. A 1 enables conversion of the corresponding channel: [14] – enable conversion on reference 1 (0 V); [13] – enable conversion on reference 0 (+10 V); [12] – enable conversion of channel 7; [11] – enable conversion of channel 6; [10] – enable conversion of channel 5; [9] – enable conversion of channel 4; [8] – enable conversion of channel 3; [7] – enable conversion of channel 2; [6] – enable conversion of channel 1; [5] – enable conversion of channel 0.
[4:1]	WO	0000	ADC read channel select: 0000 - channel 0; 0001 - channel 1; 0010 - channel 2; 0011 - channel 3; 0100 - channel 4; 0101 - channel 5; 0110 - channel 6; 0111 - channel 7; 1000 - reference 0 (+10 V); 1001 - reference 1 (0 V).
[0]	WO	0	ADC start. Writing a 1 to this bit starts conversion on channels selected with bits [14:5] (Note 1). Bit [2] of the Interrupt Status register is set to 1 when upload is complete.

Notes:
1. Selection of channels and ADC start can be performed in one access to the ADC Control register.

DAC/ADC Data Register
0x08

Bits	Type	Default	Description
[15:0]	RW	0x0000	Write operation: data to be written to DAC preload register for the channel selected in DAC control register. Read operation: conversion result from ADC channel selected in ADC control register.

Digital I/O Control Register
0x0A

Bits	Type	Default	Description
[15]	WO	0	DIO(3) interrupt condition: 0 – interrupt on a rising edge; 1 – interrupt on a falling edge.
[14]	WO	0	DIO(2) interrupt condition: 0 – interrupt on a rising edge; 1 – interrupt on a falling edge.
[13]	WO	0	DIO(1) interrupt condition: 0 – interrupt on a rising edge; 1 – interrupt on a falling edge.
[12]	WO	0	DIO(0) interrupt condition: 0 – interrupt on a rising edge; 1 – interrupt on a falling edge.
[11]	WO	0	DIO group 2 mode: 0 – input; 1 – output.
[10]	WO	0	DIO group 1 mode: 0 – input; 1 – output.
[9]	UU	X	Reserved.
[8]	WO	0	DIO group 2 interrupt condition: 0 – interrupt on a rising edge; 1 – interrupt on a falling edge.
[7:0]	RW	0x00	Write operations set the bits configured as outputs, do not affect the bits configured as inputs. Read operations return the current values of the bits configured as inputs and last written value of the bits configured as outputs. (Note 1).

Notes:
1. Enabling an interrupt on a DIO bit configured as output will result in the interrupt when the interrupt condition is met: for example, if a DIO bit is configured as output, has an interrupt configured on a rising edge and enabled, and its current state is 0, writing a 1 to this bit will generate an interrupt.

Interrupt Enable Register
0x0C

Bits	Type	Default	Description
[15]	WO	0	DIO7 interrupt enable.
[14]	WO	0	DIO6 interrupt enable.
[13]	WO	0	DIO5 interrupt enable.
[12]	WO	0	DIO4 interrupt enable.
[11]	WO	0	DIO3 interrupt enable.
[10]	WO	0	DIO2 interrupt enable.
[9]	WO	0	DIO1 interrupt enable.
[8]	WO	0	DIO0 interrupt enable.
[7]	UU	X	Reserved.
[6]	WO	0	Counter 0 interrupt enable.
[5]	WO	0	Counter 1 interrupt enable.
[4]	WO	0	Counter 2 interrupt enable.
[3]	WO	0	Counter 3 interrupt enable.
[2]	WO	0	ADC interrupt enable.
[1]	WO	0	DAC interrupt enable.
[0]	WO	0	Timer interrupt enable.

Interrupt Status Register
0x0E

Bits	Type	Default	Description
[15]	RR	0	DIO7 interrupt status.
[14]	RR	0	DIO6 interrupt status.
[13]	RR	0	DIO5 interrupt status.
[12]	RR	0	DIO4 interrupt status.
[11]	RR	0	DIO3 interrupt status.
[10]	RR	0	DIO2 interrupt status.
[9]	RR	0	DIO1 interrupt status.
[8]	RR	0	DIO0 interrupt status.
[7]	RR	0	EEPROM interface status (status only, no interrupt).
[6]	RR	0	Counter 0 interrupt status. Note 1.
[5]	RR	0	Counter 1 interrupt status. Note 1.
[4]	RR	0	Counter 2 interrupt status. Note 1.
[3]	RR	0	Counter 3 interrupt status. Note 1.
[2]	RR	0	ADC interrupt status.
[1]	RR	0	DAC interrupt status.
[0]	RR	0	Timer interrupt status.

Notes:
1. This interrupt can be generated by multiple sources. Detection of the exact interrupt source is possible through the individual interrupt status bits in the corresponding counter status register. Those bits have to be reset as well after an interrupt occurs to enable subsequent interrupt detection.

Miscellaneous Register
0x10

Bits	Type	Default	Description
[15:1]	UU	X	Reserved.
[0]	RW	0	LED control. A 0 turns the LED on, a 1 turns it off.

Counter Preload/Data Register low word
0x12 – counter 0,
0x1A – counter 1,
0x22 – counter 2,
0x2A – counter 3.

Bits	Type	Default	Description
[15:0]	RW	0x0000	Write operation: Low word of the preload register selected by bit [14] of Counter Mode Register. Read operation: Low word of latched counter data.

Counter Preload/Data Register high word
0x14 – counter 0,
0x1C – counter 1,
0x24 – counter 2,
0x2C – counter 3.

Bits	Type	Default	Description
[15:0]	RW	0x0000	Write operation: High word of the preload register selected by bit [14] of Counter Mode Register. Read operation: High word of latched counter data.

Counter Mode Register

0x16 – counter 0,
0x1E – counter 1,
0x26 – counter 2,
0x2E – counter 3.

Bits	Type	Default	Description
[15]	UU	X	Reserved.
[14]	WO	0	Preload register select: 0 – writes to Preload Register directed to PR0; 1 – writes to Preload Register directed to PR1.
[13]	WO	0	Output register latch control: 0 – latch on read (Note 1); 1 – latch on event (Note 2).
[12]	WO	0	Count direction control: 0 – quadrature (dependent on CLKA-CLKB relative phase); 1 – software control.
[11]	WO	0	Count direction if [12]=1, no effect if [12]=0: 0 – up; 1 – down.
[10:9]	WO	00	Clock source: If [12]=0: 00 – quadrature x1 (CLKA↑ counting up, CLKA↓ counting down); 01 – quadrature x2 (both edges of CLKA); 1X – quadrature x4 (both edges of both CLKA and CLKB). If [12]=1: 00 – CLKA↑; 01 – CLKA↓; 10 – internal clock; 11 – internal clock ÷ 2.
[8:7]	WO	00	Count Enable control: 00 – count disabled; 01 – count enabled; 10 – hardware Count Enable (configured with [6:5]); 11 – hardware Count Enable (configured with [6:5]), inverted polarity.
[6:5]	WO	00	Hardware Count Enable source: 00 – CEN; 01 – INDEX; 10 – INDEX ↑ to ↓; 11 – NOT RCAP.
[4:2]	WO	000	Auto load and reset RCAP (can be OR'ed): [4] – INDEX↑; [3] – INDEX↓; [2] – RO.
[1]	WO	0	COUT polarity: 0 – normal; 1 – inverted.
[0]	WO	0	COUT source select: 0 – RCAP; 1 – RTGL.

Notes.
1. In “Latch on read” mode data from the counter is latched on the read access to the Counter data low word register. Thus the low word has to be always read first in this mode.
2. In “Latch on event” mode data from the counter is latched by the event(s) selected with bits [12:10] of Counter Control/Status register.

Counter Control/Status Register

0x18 – counter 0,
0x20 – counter 1,
0x28 – counter 2,
0x30 – counter 3.

Bits	Type	Default	Description
[15]	WO	0	Counter reset. Writing a 1 resets the counter and RTGL to 0.
[14]	WO	0	Counter load. Writing a 1 loads a counter from PR0.
[13]	WO	0	Counter arm. Writing a 1 enables count to start at the rising edge of Count Enable signal (only relevant when Hardware Count Enable source is set to “INDEX↑ to ↓”, bits [6:5] of Mode Register).
[12:10]	WO	000	Latch event select: [12] – latch data on interrupt timer expiration; [11] – latch data on INDEX↑; [10] – latch data on INDEX↓.
[9:6]	WO	0000	Interrupt enable. Writing a 1 enables an interrupt from the corresponding event (Note 1): [9] – RO; [8] – INDEX↑; [7] – INDEX↓; [6] – ERROR.
[5]	RO	0	INDEX real time status. Write has no effect.
[4]	RO	0	COUT real time status. Write has no effect.
[3:0]	RR	0000	Captured events status bits (Note 2). Writing a 1 resets corresponding signal and status bit to 0: [3] – RCAP; [2] – ICAP+; [1] – ICAP-; [0] – ECAP.

Notes:
1. Interrupt for a particular counter has to be enabled in Interrupt Enable Register as well.
2. All bits in this group are captured events, i.e. they are set to 1 when a corresponding event occurs, and keep this value until reset to 0. Corresponding bit in the Interrupt Status Register is set as soon as any of the captured events status bits is set to 1. The bit(s) set to 1 must be reset to 0 to enable subsequent interrupt detection.

EEPROM Data Register

0x32

Bits	Type	Default	Description
[15:0]	RW	0x0000	EEPROM data. Read accesses return the last value read from EEPROM.

EEPROM Command/Status Register

0x34

Bits	Type	Default	Description
[8:3]	WO	000000	EEPROM address.
[2:1]	WO	00	Must be set to 10 for read access.
[0]	WO	0	EEPROM access start bit. Writing a 1 to this bit starts EEPROM access. The bit in the Interrupt Status Register is set to 1 when access is complete.

Notes:

1. Read access to the EEPROM Command/Status register returns a value of 0x526X, where X is a firmware revision number.

Specifications

Parameter	Value	Units	Notes
D/A Converter			
Number of channels	4		
Resolution	16	bits	
Upload time, max	8	µs	
Settling time, max	100	µs	
Output range, min	±10	V	
Max output current	±2	mA	Each channel
A/D Converter			
Number of channels	8		
Resolution	16	bits	
Input range, min	±10	V	
Conversion time, no channel switching, max	10	µs	
Conversion time, with channels switching, max	25	µs	
Noise, max	3	LSB	1σ
Counters			
Number of counters	4		
Counter width	24	bits	
Inputs (differential or single-end)	RS–422/TTL/CMOS		ClkA, ClkB, Index
Inputs (single-end)	TTL/CMOS		Clock Enable, 10K pull up to +5V
External clock, max	TBD	MHz	Quad mode, each phase
Digital outputs			
Output current	±20	mA	10K pull up to +5V
Watchdog timer solid state relays			
Continuous current	150	mA	
Maximum voltage	400	V	
Insulation voltage	1500	V	RMS
Power			
Supply voltage	5 ± 5%	V	
Supply current	TBD	mA	
Temperature range			
Operating	0- +70	°C	
Storage	-55- +125	°C	