PO3030K Data sheet
(Brief)

Pixelplus Co.,Ltd

PO3030K
1/6.2 Inch VGA Single Chip CMOS IMAGE SENSOR

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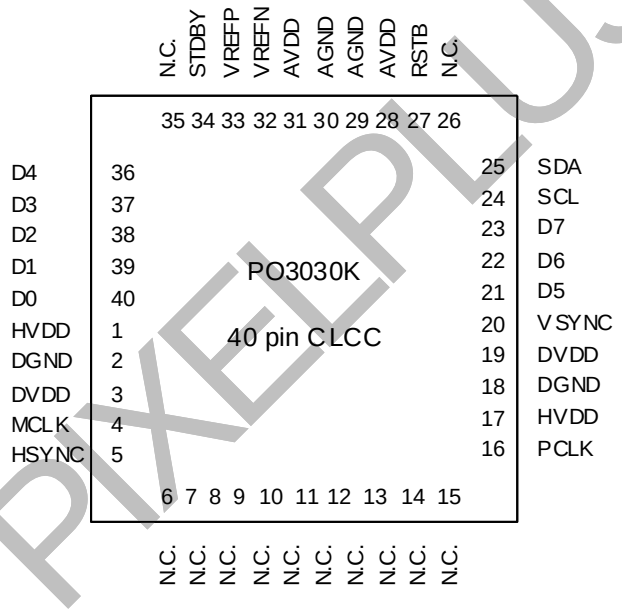
CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

§ This document is an initial draft. It will be revised on without prior notice.
Contact Pixelplus for up-to-date information.

Features

- 1/6.2 inch 640 X 480 effective pixel array with color filters and micro-lens.
- Power supply 1.8V for core and 1.8 ~ 3.3V for I/O.
- Output formats : 8bit YCbCr / 9Bit Bayer data / 5:6:5 RGB / 8bit Y
- 30 frames/sec progressive scan @27 MHz master clock.
- Image processing on chip : lens shading, gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, contrast stretch, color saturation, white balance, exposure control and back light compensation.
- Still image capture with electrical shutter.
- Frame size, window size and position controllable through a serial interface bus.
- VGA / QVGA / QQVGA Scaling.
- Horizontal / Vertical mirroring.
- 50Hz, 60Hz flicker cancellation.
- Package : 40 pin CLCC, 32 pin CSP



< Figure. 1> Pin Diagram

Table 1. Typical Parameters

Total Pixel Array	648 X 488
Pixel Size	3.6um X 3.6um
Image Area	2.30 mm X 1.72 mm
Clock Rate	27 MHz (Max.)
Frame rate	Variable up to 30fps
Dark Current	TDB nA/㎠
Sensitivity	TDB V/Lux.sec @15fps,IR cut filter
Saturation Level	TDB mV
Conversion Gain	TDB μV/electrons
Fill Factor	40 %
Supply voltage	1.8~3.3V I/O,1.8V Core
Power consumption	TDB mW @15fps, active
	TDB uW @standby
Operation Temp.	TDB ℃
Dynamic Range	TDB dB
Package	40 pin CLCC, 32 pin CSP

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PIN Descriptions

Pin No.	Name	I/O Type	Functions / Descriptions
1	HVDD	P	Digital vdd for I/O : DC 1.8~3.3V. Voltage range for all output signals is 0V ~ HVDD.
2	DGND	P	Digital ground. Core and I/O circuits share the ground pads.
3	DVDD	P	Digital vdd for core logic : 1.8 V DC. 100nF capacitor to DGND.
4	MCLK	I	Master clock input pad.
5	HSYNC	O	Horizontal synchronization pulse. HSYNC is high (or low) for the horizontal window of interest. It can be programmed to appear or not outside the vertical window of interest.
6 - 15	N.C.	-	No Connection.
16	PCLK	O	Pixel clock. Data can be latched by external devices at the rising or falling edge of PCLK. The polarity can be controlled anyway.
17	HVDD	P	Digital vdd for I/O : DC 1.8~3.3V. Voltage range for all output signals is 0V ~ HVDD.
18	DGND	P	Digital ground. Core and I/O circuits share the ground pads.
19	DVDD	P	Digital vdd for core logic : 1.8 V DC. 100nF capacitor to DGND.
20	VSYNC	O	Vertical sync : Indicates the start of a new frame.
21	D5	O	Bit 5 of data output.
22	D6	O	Bit 6 of data output.
23	D7	O	Bit 7 of data output.
24	SCL	I	I2C serial clock input.
25	SDA	I/O	I2C serial data bus.
26	N.C.	-	No Connection.
27	RSTB	I	System reset must remain low for at least 8 master clocks after power is stabilized. When the sensor is reset, all registers are set to their default values.
28	AVDD	P	Analog vdd : 1.8V DC. 100nF capacitor to AGND.
29	AGND	P	Analog ground.
30	AGND	P	Analog ground.
31	AVDD	P	Analog vdd : 1.8V DC. 100nF capacitor to AGND.

Table 2-1. PIN Descriptions

Pin No.	Name	I/O Type	Functions / Descriptions
32	VREFN	O	ADC reference voltage. 100nF capacitor to AGND. ADC assumes VREFP – VREFN is the minimum input voltage that will be converted to 1FFh.
33	VREFP	O	ADC reference voltage. 100nF capacitor to AGND.
34	STDBY	I	Power standby mode. When STDBY='1' there's no current flow in any analog circuit branch, neither any beat of digital clock. D<8:0> and PCLK, HSYNC, VSYNC pins can be programmed to tri-state or all '1' or all '0'. But it is possible to control internal registers through I2C bus interface in STDBY mode. All registers retain their current values.
35	N.C.	-	No Connection.
36	D4	O	Bit 4 of data output.
37	D3	O	Bit 3 of data output.
38	D2	O	Bit 2 of data output.
39	D1	O	Bit 1 of data output.
40	D0	O	Bit 0 of data output.

Table 2-2. PIN Descriptions

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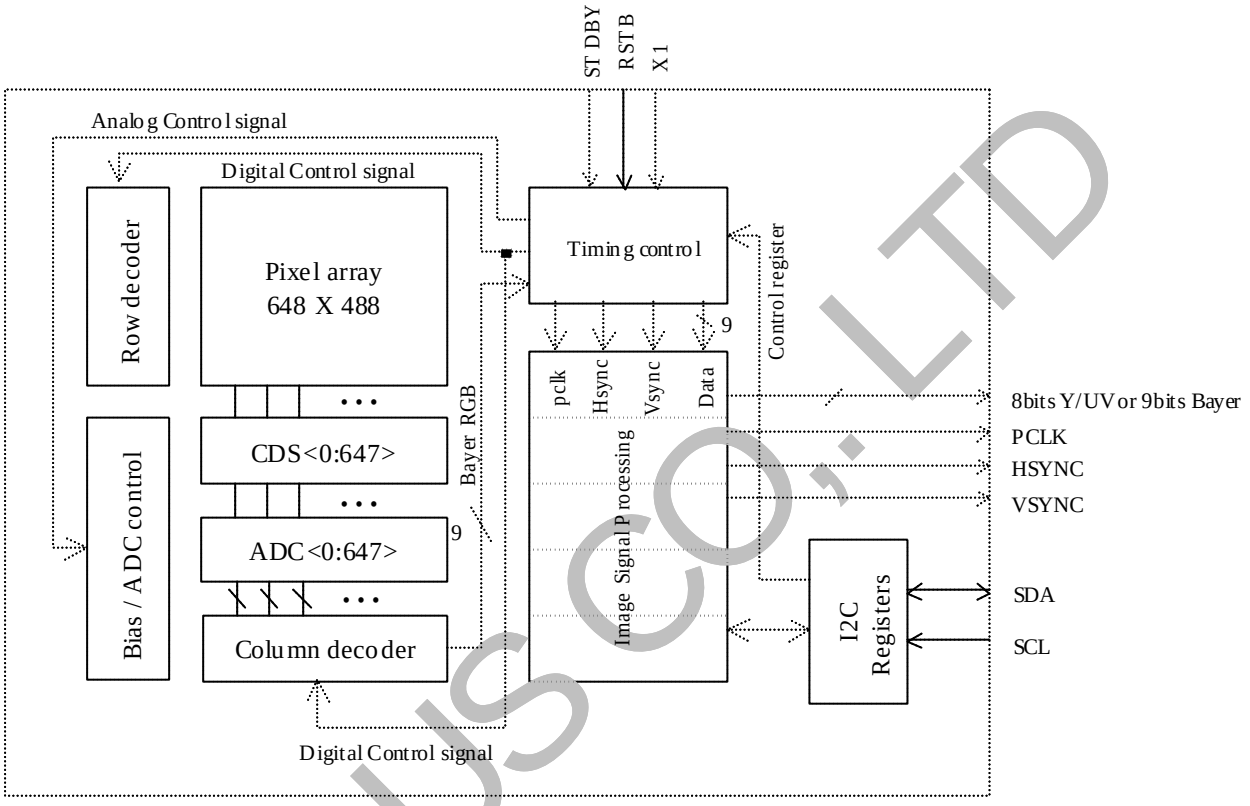
Block Diagram



< Figure. 2 > Block Diagram

PO3030K has 648 x 488 effective pixel array and column/row driver circuits to read out the pixel data progressively. CDS circuit reduces noise signals generated from various sources mainly resulting from process variations. Pixel output is compared with the reset level of its own and only the difference signal is sampled, thus reducing fixed error signal level. Each of R, G, B pixel output can be multiplied by different gain factors to balance the color of images in various light conditions. The analog signals are converted to digital forms one line at a time and 1 line data are streamed out column by column. The Bayer RGB data are passed through a sequence of image signal processing blocks to finally produce YCbCr 4:2:2 output data. Image signal processing includes such operations as gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, contrast stretch, color saturation, white balance, exposure control and back light compensation. Internal functions and output signal timing can be programmed simply by modifying the register files through I^2C serial interface.